Intel® Pentium® M Processor, Intel® 855GME Chipset and Intel® 6300ESB ICH Development Kit

User's Manual

July 2005

Order Number: 301176-002

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Revision History

Date	Revision	Description
March 2004	001	Initial public release of this document.
July 2005	002	General document clean-up. Updates include: Section 1.5: Added relevant documents. Section 2.1: Removed reference to kit containing a power supply. Section 2.2: Updated board features summary. Removed reference to 24-bpp LVDS panel support. Updated System I/O section. Removed section 2.2.5. Section 2.6: Updated Jumper Settings table and moved table to Section 4.3. Section 3.1: Replaced Figure 2 with updated block diagram. Section 3.3: Updated system features section. Corrected errors in System I/O section. Figure 3 (Back Panel I/O Connectors) was corrected and moved to Section 4.7. Added AGP/ADD Connector, LVDS Connector, and AC'97 Audio sections. Updated System Clocks section. Chapter 4: Replaced Board Layout Diagram with corrected version. Corrected Expansion Slots and Sockets section. Added missing tables. Corrected On-Board Connectors section. Added missing tables. Added Jumpers section. Added On-board Headers section. Appendix A: Replaced Fab C, Rev 0 schematics with Fab C, Rev 3 version.

About This Manual 1

This manual describes how to set up and use the evaluation board and other components included in your Intel® Pentium® M Processor, Intel® 855GME Chipset and Intel® 6300ESB ICH Development Kit.

1.1 Content Overview

Chapter 1, “About This Manual” – This chapter contains a description of conventions used in this manual and instructions for obtaining literature and contacting customer support.

Chapter 2, “Getting Started” – Provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, “Theory of Operation” – This chapter provides information on the system design.

Chapter 4, “Hardware Reference” – This chapter provides a description of jumper settings and functions, and pinout information for each connector.

Chapter 5, “BIOS Overview”– This chapter provides information on BIOS setup and configuration.

Appendix A, “Schematics” – This appendix contains the schematics for the evaluation board.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in *italics*. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper- or lowercase.
Numbers	Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character H. A zero prefix is added to numbers that begin with A through F. For example, FF is shown as 0FFH. Decimal and binary numbers are represented by their customary notations. That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter B is added for clarity.
Signal Names	Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (n). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CSn#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).
Units of Measure	The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
GHz	gigahertz
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

1.3 Technical Support

1.3.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

1.3.1.1 Online Documents

Product documentation is provided online in a variety of web-friendly formats at:

http://developer.intel.com/design/intarch/devkits/index.htm

1.3.2 Additional Technical Support

If you require additional technical support, please contact your field sales representative or local distributor.

1.4 Product Literature

You can order product literature from the following Intel literature centers.

1-800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

1.5 Related Documents

For more information, contact your local Intel representative.

Table 1. Related Documents

Document	Intel Order Number	Location
Intel® Pentium® M Processor Datasheet	252612	http://developer.intel.com/design/intarch/
Intel® Pentium® M Processor on 90nm Process with 2-MB L2 Cache Datasheet	302189	http://developer.intel.com/design/intarch/
Intel® 855GME Chipset and Intel® 6300ESB I/O Controller Hub Embedded Platform Design Guide	300669	http://developer.intel.com/design/intarch/
Intel® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet	252615	http://developer.intel.com/design/intarch/
Intel® 855GM/GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update	253572	http://developer.intel.com/design/intarch/
Intel® 855GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update Addendum	274004	http://developer.intel.com/design/intarch/
Intel® 855GME and Intel® 852GME Chipset Memory Controller Hub (MCH) Thermal Design Guide for Embedded Applications	273838	http://developer.intel.com/design/intarch/
Intel® 6300ESB I/O Controller Hub Datasheet	300641	http://developer.intel.com/design/intarch/
Intel® 6300ESB I/O Controller Hub (ICH) Specification Update	300884	http://developer.intel.com/design/intarch/
Intel® 6300ESB I/O Controller Hub (ICH) Thermal and Mechanical Design Guide	300682	http://developer.intel.com/design/intarch/
ITP700 Debug Port Design Guide	249679	http://developer.intel.com/design/intarch/

Getting Started 2

This chapter identifies the Intel® Pentium® M Processor, Intel® 855GME Chipset and Intel® 6300ESB I/O Controller Hub (ICH) Development Kit's key components, features and specifications. It also describes how to set up the board for operation.

2.1 Overview

The development kit contains a baseboard with a Pentium M processor with 1Mbyte L2 cache, 855GME chipset, 6300ESB ICH, and other system board components and peripheral connectors. Various software and documentation are also included in the kit.

Note: This manual assumes that you are familiar with the basic concepts involved with installing and configuring hardware for a PC or server system.

2.2 Evaluation Board Features

The evaluation board features are summarized below:

2.2.1 Processor

- Optimized for the Intel® Pentium® M Processor and Intel® Celeron® M Processor in 478-pin µ-FCPGA package with 400 MHz FSB.

2.2.2 Intel® 855GME GMCH with Intel® 6300ESB ICH Chipset

- Supports the 855GME chipset with 400 MHz system bus
  - — Supports 333/266/200 MHz unbuffered DDR with a maximum of two double-sided DIMMs for a total of 2GB of system memory
  - — ECC support in integrated graphics mode only
- Supports the 6300ESB ICH

2.2.3 Flash System BIOS ROM

- Intel® 82802AC Firmware Hub (FWH)
- 8 Mbit
- AMI* system BIOS

2.2.4 System I/O

- Two PCI slots
- Two PCI-X slots
- Four USB 2.0 ports (Two in the back and two in the front)
- Two Serial ATA connectors
- Two Parallel ATA connectors
- Two Serial ports from 6300ESB ICH
- One Serial port header from Super I/O
- One Parallel port from Super I/O
- Two PS/2 ports from Super I/O
- One Floppy connector from Super I/O
- Line IN, Line Out, CD IN and MIC IN connectors
- VGA Connector
- AGP/ADD Connector
- LVDS Connector

2.3 Included Hardware

The following hardware is included in the development kit:

- Evaluation board (baseboard) with battery
- BIOS Image from American Megatrends* (FWH installed on board)
- One Pentium M processor with 1 Mbytes L2 cache at 1.6 GHz with 400 MHz FSB (installed on board)
- One processor fansink thermal solution and metal attachment bracket
- One MCH heatsink and attachment clip
- One 128 Mbytes DDR DIMM
- 80-pin IDE cable for the hard disk drive (cable will support two IDE devices)

2.4 Software Key Features

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in your development kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using tools that work with other third party products must have licensed those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third party vendors.

2.4.1 AMIBIOS*

The evaluation board is pre-installed and licensed with a copy of AMIBIOS8* from American Megatrends*.

2.5 Before You Begin

Table 2 presents the additional hardware you may need for your development kit.

Table 2. Additional Hardware

Component	Description
VGA Monitor	You can use any standard VGA or greater resolution monitor.
Keyboard	You can use a keyboard with a PS/2 style connector or adapter. A USB keyboard can also be used.
Mouse	You can use a mouse with a PS/2 style connector or adapter. A USB mouse can also be used.
IDE Devices	You can connect up to four IDE devices to the evaluation board. One IDE hard drive and cable are included in your kit. The cable accommodates the included hard drive and one other IDE device, such as a CD-ROM drive or another hard drive.
SATA Devices	You can connect up to two SATA drives to the evaluation board. No SATA drives or cables are included in the development kit.
Floppy Drive	You can connect up to two floppy drives to the connector on the evaluation board. No floppy drives or cables are included in the development kit.
Video Adapter	You can use the on-board video adapter supplied with your kit, or you may install your own PCI or AGP video adapter. You must procure and install the correct drivers for any additional video adapters.
Network Adapter	An Ethernet controller is not included in this development kit. An external controller is required to connect to your network; however you are responsible for installing the correct drivers for any network cards.
Other Devices and Adapters	The evaluation board behaves much like a standard PC motherboard. Many PC-compatible peripherals can be attached and configured to work with the evaluation board. For example, you may want to install a sound card or additional network adapters. You are responsible for procuring and installing any drivers required for additional devices.
ATX Power Supply	You must use an ATX 12 V power supply with a minimum of 300 W support.

2.6 Setting up the Evaluation Board

Once you have gathered the hardware described in the last section, follow the steps below to set up your development kit. This manual assumes you are familiar with basic concepts involved with installing and configuring hardware for a PC or server system.

1. **Ensure a safe work environment.** Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge, which may cause product failure or unpredictable operation.

Caution: Connecting the wrong cable or reversing a cable may damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

Caution: Missing AT mounting hole under PCI-X connection. Use caution if mounting in a chassis.

2. **Verify kit contents.** Inspect the contents of your kit, and ensure that everything listed in Section 2.3 is included. Check for damage that may have occurred during shipment. Contact your Intel sales representative if any items are missing or damaged.
3. **Gather tools.** You will need a Phillips-head screwdriver and a 6/32-inch hex wrench for installation.
4. **Check jumper settings.** Verify that the following jumpers are set in their default state (see Table 10 on page 38).
5. **Verify installed hardware.** Make sure the following hardware is populated on your evaluation board:
   - One Pentium M processor in socket U8D1
   - BIOS FWH in socket U1H1
   - Battery in battery holder BH1G1

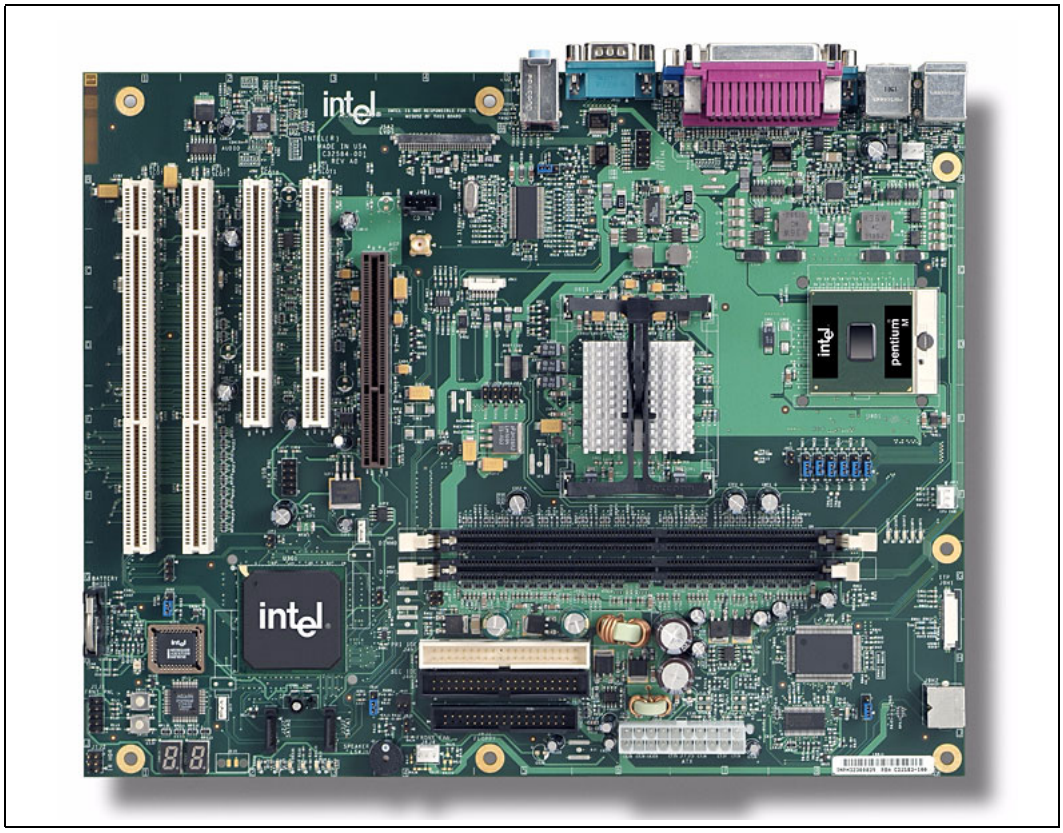
   Note: The above hardware should have been correctly installed at the factory. If they are not installed correctly, DO NOT power on the board. Correctly re-install the components before proceeding. If you suspect that any of the kit components have been damaged, contact your Intel field sales representative or local distributor for assistance.

6. **Install fansinks.** You must install a fansink on the processor. Place the white gasket on the heat sink retention mechanism. From the back of the board feed the heat sink retention mechanism lugs up through the board. Apply an even amount of thermal grease on the die of the Pentium M processor. Place the fansink on top of the processor, fitting it onto the retention mechanism lugs. Slide the fansink to lock it onto the retention mechanism lugs. Rotate the heatsink clockwise to apply slight pressure onto the die. Connect the three-pin fansink power connector to connector J9F1 on the evaluation board.

Caution: Applying excess pressure may cause the die to crack.

7. **Install memory.** Your kit includes one 128 Mbyte DIMM. Install the DIMM in memory slot J4G1 or J4G2. To install, ensure the tabs on the slot are open, or rotated outward from the slot. Line up the DIMM above the slot (the DIMM is keyed so that it only fits in the slot in one orientation). Firmly, but carefully, insert the DIMM into the slot until the tabs close.

Figure 1. Assembled Board, Top View



8. **Install storage devices.** There are two IDE connectors on the evaluation board. Each connector supports two IDE devices—a master and a slave. The kit includes one IDE hard drive.

   For a correct boot-up of the system, ensure that the included hard drive is installed as the primary master.

   Note: Master/slave settings are determined by a jumper on each IDE device. Consult the device label/documentation to verify that the jumper is set correctly for the configuration you choose.

A CD-ROM drive or additional hard drive may be installed as a primary slave device or secondary master/slave device.

To install the included hard drive on the evaluation board:

a. Verify that the jumper on the hard drive is set correct for single or master, depending on your configuration.

b. Connect the short end of the IDE cable to the IDE connector J4H2 on the board. Ensure that the tracer on the cable is aligned with pin 1 of the connector.

c. Connect the middle connector of the cable to the hard drive. Again, ensure that the cable tracer is aligned with pin 1 of the connector.

Note: Failure to properly align the IDE cable may damage the evaluation board and/or the hard drive.

d. Connect a large four-pin power connector from the power supply to the hard drive.

e. Install the CD-ROM drive (optional). A CD-ROM drive is not included in the kit and is not required, but you may find it useful in loading additional software. You must furnish your own CD-ROM drive. To install it on the evaluation board:

— Verify that the jumper on the CD-ROM drive is set for slave.

— Connect the unused end of the IDE cable you already attached to the evaluation board to the CD-ROM drive. Ensure that the cable tracer is aligned with pin 1 of the CD-ROM drive connector.

— Connect a large four-pin power connector from the power supply to the CD-ROM drive.

f. Install the floppy drive (optional). A floppy disk drive is not included in your kit and is not required, but you may find it useful in loading additional software. You must furnish your own floppy drive(s) and cable. To install a floppy drive on the evaluation board:

— Connect the floppy cable to the floppy connector J4J2. Ensure that the tracer on the cable is aligned with pin 1 of the connector.

— Connect the other end of the floppy cable to the floppy drive. Ensure that the tracer on the cable is aligned with pin 1 of the connector.

— Connect a power cable to the floppy drive.

9. **Connect the monitor.** Connect the monitor cable to the VGA port.

10. **Connect the keyboard and mouse.** Connect a PS/2 mouse and keyboard to the stacked PS/2 connector on the evaluation board. The top connector is for the mouse, and the bottom is for the keyboard. Alternatively, you may plug a USB keyboard and a USB mouse into one or both of the USB connectors on the evaluation board. Note that a legacy (PS/2) keyboard may be required for BIOS setup.

11. **Connect the power supply.** Make sure the power supply is turned off and unplugged. Connect the ATX power supply cables to connector J7J5 on the evaluation board. Next, plug the power cord into the power supply and the wall.

12. **Power up the system.** Turn on the monitor, then turn on the evaluation board. The on-board power on/off button is located at SW1J1. The on-board reset button is located at SW1H1.

Caution: Ensure that the fansink on the processor is operating. If not, turn off the power immediately and verify that the fansink is connected to the board correctly (see Step 6). If the fansink is not operating, contact your Intel field sales representative or local distributor.

2.7 Configuring the BIOS

An AMIBIOS* is pre-loaded on the evaluation board. You may need to make changes to the BIOS to enable hard disks, floppy disks and other supported features. You may use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. On first boot-up of the system, you may want to use the BIOS setup program to verify the date/time and boot device.

Note: ***Pressing the Delete key during boot causes the system to enter into the BIOS setup program.***

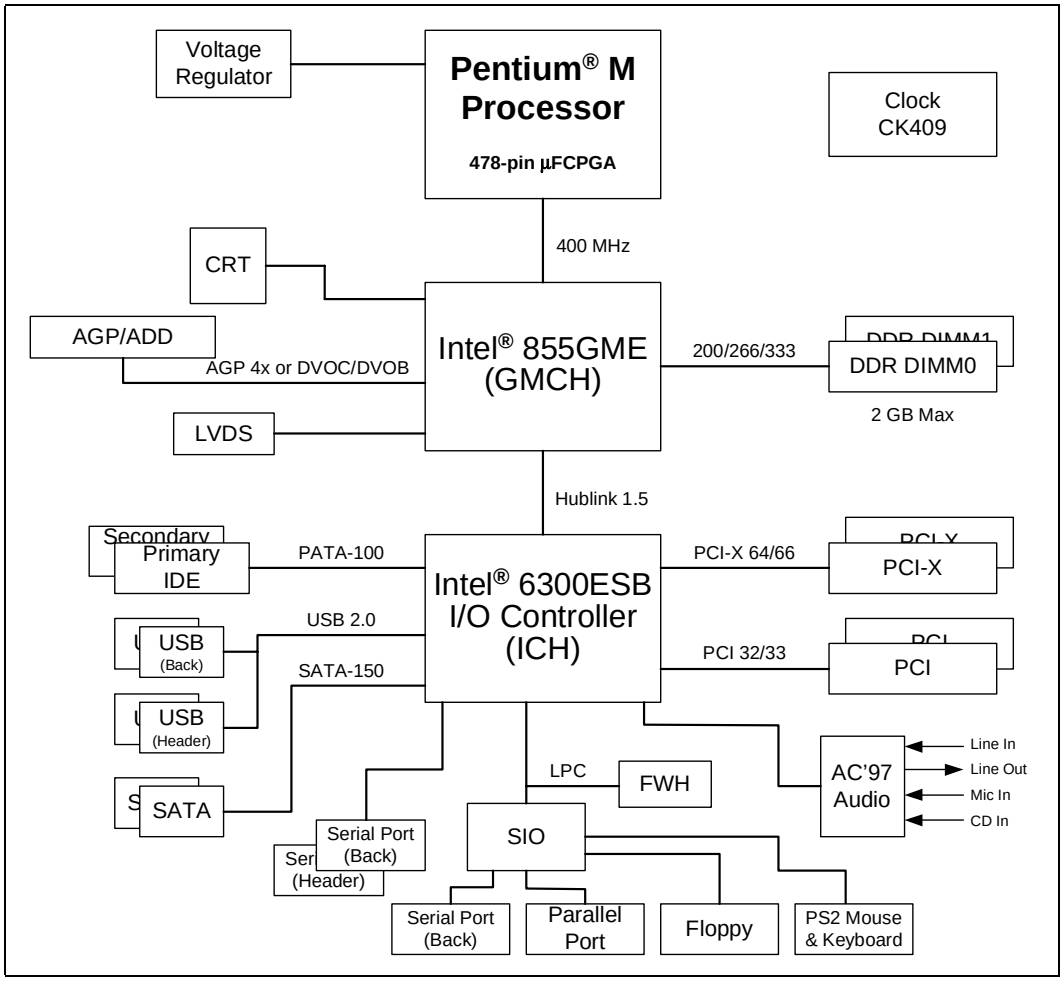
Refer to Chapter 5, “BIOS Overview” for more information.

BIOS updates can be obtained by contacting your local field sales representative or local distributor.

Theory of Operation 3

3.1 Block Diagram

Figure 2. Block Diagram - Evaluation Board Overview



3.2 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits may be expected to meet their specified performance requirements. Operation outside the functional limit may degrade system performance and cause reliability problems.

The development kit is shipped with fansink thermal solutions to be installed on the processor. This thermal solution has been tested in an open air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

3.3 System Features

Supported Processors:

- Intel® Pentium® M Processor
- Intel® Pentium® M Processor on 90nm Process with 2-MB L2 Cache
- Intel® Celeron® M Processor
- 400 MHz Front Side Bus (FSB) support

Chipset:

- Intel® 855GME Chipset GMCH with 400 MHz FSB support
- Intel® 6300ESB ICH with PCI-X 66 MHz support

Memory:

- One channel unbuffered DDR 200/266/333 MHz (PC1600/2100/2700) support
- Two DIMMs, 1 GByte maximum per DIMM for 2 GByte maximum total memory
- 128 Mbit, 256 Mbit, and 512 Mbit DDR device technology support
- ECC supported (in integrated graphics mode)

Graphics:

- Integrated graphics (CRT, LVDS, DVOB/C)
- LVDS supports data format up to 18-bpp
- AGP 4X 1.5V support

Expandability:

- Two PCI slots
- Two PCI-X slots
- Four USB 2.0 ports (Two in the back and two in the front)
- Two Serial ATA connectors
- Two Parallel ATA connectors
- Two Serial ports from 6300ESB ICH
- One Serial port header from Super I/O
- One Parallel port from Super I/O
- Two PS/2 ports from Super I/O
- One Floppy connector from Super I/O

Audio:

- AC ‘97 integrated audio
- Line IN, Line Out, CD IN and MIC IN connectors

3.3.1 Intel® Pentium® M Processor

The Pentium M processor is a high performance, lower voltage processor with several micro-architectural enhancements over existing Intel mobile processors. Some key features of the Pentium M processor micro-architecture include:

- Dynamic execution
- Data pre-fetch logic
- 400 MHz source-synchronous FSB
- On-die 1 Mbyte second level (L2) cache with Advanced Transfer Cache Architecture
- Streaming SIMD Extensions 2 (SSE2)
- Enhanced Intel SpeedStep® technology.

The FSB uses source-synchronous transfer of address and data to improve performance and enable addressing at 2x the system bus frequency and data transfers at 4x the system bus frequency of 100 MHz. This allows the 400 MHz system bus support to transfer data at 3.2 Gbytes/s.

The Pentium M processor includes the advanced micro-architecture features described in the following sections.

3.3.1.1 Architectural Features

- On-die primary 32 Kbyte instruction cache and 32 Kbyte write-back data cache
- On-die 1 Mbyte L2 cache
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Enhanced Intel SpeedStep technology to enable real-time dynamic switching between multiple voltage and frequency points
- Supports host bus Dynamic Bus Inversion (DINV)
- Dynamic power down of data bus buffers
- BPRI# control to disable address/control buffers

3.3.1.2 Packaging/Power

- 479-ball Micro-FCBGA packages
- 478-pin Micro-FCPGA packages
- $V_{CC\text{-}CORE}$: 1.484 V (highest frequency mode) to 0.956 V (lowest frequency mode)
- VCCA (1.8 V)
- VCCP (1.05 V)

3.3.1.3 Enhanced Intel® SpeedStep® Technology

The Pentium M processor features Enhanced Intel SpeedStep technology. Unlike current implementations of Enhanced Intel SpeedStep technology, this technology may enable the processor to switch between multiple frequency and voltage points instead of two. This may enable superior performance with optimal power savings. Switching between states may be software controlled, unlike previous implementations where the GHI# pin is used to toggle between two states. Following are the key features of Enhanced Intel SpeedStep technology:

- Multiple voltage/frequency operating points provide optimal performance at the lowest power. A subset of available operating points may be selectable to provide maximum flexibility.
- Voltage/Frequency selection may be software controlled by writing to processor MSRs (Model Specific Registers) thus eliminating chipset dependency.
  - When the target frequency is higher than the current frequency, V_{CC} is ramped up by placing a new value on the VID pins and the PLL then locks to the new frequency.
  - When the target frequency is lower than the current frequency, the PLL locks to the new frequency and then the V_{CC} is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. When a previous transition is in progress, the new transition is deferred until its completion.
- The processor may control voltage ramp rates internally to ensure glitch-free transitions.
- Low transition latency and large number of transitions possible per second.
  - Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition.
  - The bus protocol (BNR# mechanism) is used to block snooping during the transition.
- No bus master arbiter disable required prior to transition and no processor cache flush necessary.
- Improved thermal throttling:
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor may automatically perform a transition to a lower frequency/voltage specified in a software-programmable MSR.
  - The processor waits for a time period (target value is 1 ms). When the die temperature is down to acceptable levels an up transition to the previous frequency/voltage point occurs.
  - An interrupt is generated for up and down throttling transitions, enabling better system level thermal management.

3.3.2 Intel® 855GME GMCH with Intel® 6300ESB ICH Chipset

The 855GME chipset GMCH component provides the processor interface, SDRAM interface, display interface, and hub interface in an 855GME chipset platform. The Intel 855GME chipset GMCH is optimized for the Pentium M processor. It supports a single channel of DDR memory. The 855GME chipset GMCH contains advanced power management logic. The 855GME chipset platform supports the 6300ESB ICH, which contains many enhancements to the Intel® ICH4 and Intel® ICH5.

3.3.2.1 Intel® 855GME Graphics Memory Controller Hub (GMCH)

The 855GME chipset contains the following functionality:

- Optimized for Pentium M processor and Intel® Celeron® M Processor
  - Eight-deep in-order queue
  - AGTL+ bus driver technology with integrated AGTL+ termination resistors and low voltage operation (V_{TT} = 1.05V)
  - Supports Enhanced Intel SpeedStep technology
  - Support for DPWR# signal to Pentium M processor for FSB power management
- Supports a single channel of DDR SDRAM memory
  - System memory supports DDR200/266/333 MHz (SSTL_2) DDR SDRAM
  - DDR SDRAM devices with densities of 128-Mbit, 256-Mbit, and 512-Mbit technology
  - Up to 2 GBytes (512-Mbit technology) with two DIMMs
- Integrated graphics capabilities:
  - Display Core frequency at 133 MHz, 200 MHz, or 250 MHz
  - Render Core frequency at 100 MHz ,133 MHz, 166 MHz, 200 MHz, or 250 MHz
  - Provides supports four display ports: one progressive scan analog monitor, dual channel LVDS interface and two DVO ports.
- AGP 4x (1.5V only)
- 732-pin Micro-FCBGA package

3.3.2.2 Intel® 6300ESB I/O Controller Hub

The 6300ESB ICH is designed for a variety of processors/memory controller hubs and contains enhancements to the Intel ICH4 and Intel ICH5.

Features:

- PCI, PCI-X, USB2.0, ATA100, SATA, Watch Dog Timer (WDT)
- Hub Interface 1.5
- Serial Interface Unit
- Port 60/64 emulation
- Allows user to boot without Super I/O
- 37 GPIOs including four high drive and five blinking
- AC’97 integrated audio

3.3.3 Intel® 82802AC Firmware Hub (FWH)

A socketed 8 Mbit FLASH device is used to store system BIOS and video BIOS, as well as an Intel® Random Number Generator (RNG). A bootblock locking jumper is provided to allow a mechanical means of protecting the bootblock BIOS firmware. All BIOS programming is controlled via software

FWH Features:

- 32-pin PLCC package

- 8-Mbit flash memory
- Symmetrically-blocked flash memory array (64 Kbyte)
- Pin and register-based block locking
- Integrated hardware RNG
- Single-byte read/write
- Five GPIs

3.3.4 Boot ROM

The system boot ROM is installed on the Intel® 82802AC FWH device, socketed at U1H1. The FWH is addressable on the LPC bus off the 6300ESB ICH.

3.3.5 System I/O

The evaluation board contains the following I/O devices.

- Floppy controller support
- Primary and secondary IDE interface (supports four drives)
- Three serial ports (two on the back panel and one on the front header)
- One parallel port
- Four USB ports (two on the back panel, two on the front header)
- AGP/ADD connector
- VGA port
- LVDS connector
- AC'97 specification compliant audio
- Line Out, Line IN, CD IN and MIC IN connectors
- PS/2-style keyboard and mouse ports
- Two PCI Slots
- Two PCI-X Slots
- WDT
- Two SATA connectors

Refer to Table 5, "Expansion Slots and Sockets" on page 32 for expansion slots and sockets, Table 10, "Jumpers and Jumper Functions" on page 38 for locations of jumpers, Table 12, "On-Board Connectors" on page 39 for on-board connectors, Table 19, "On-Board Headers" on page 44 for on-board headers, and Figure 4, "Peripheral Connectors" on page 46 for locations of back-panel connectors.

3.3.5.1 Floppy Disk Drive Support

One 34-pin floppy connector is provided on the evaluation board, which will support up to two floppy drives.

3.3.5.2 IDE Support

The evaluation board supports both a primary and secondary IDE interface through two 40-pin IDE connectors. PRI IDE is the primary interface and SEC IDE is the secondary interface.

There are two IDE channel connectors: primary and secondary. Each channel allows two IDE devices per channel. Supports UltraATA/33/66/100 interfacing.

3.3.5.3 RS-232 Serial Port

The evaluation board provides three built-in serial ports, two from the 6300ESB ICH and one from the Super I/O device.

3.3.5.4 IEEE 1284 Parallel Port

One 25-pin DSUB IEEE 1284 Standard/EPP/ECP parallel port is provided on the evaluation board.

3.3.5.5 USB Ports

The evaluation board contains two UHCI Host Controllers and one EHCI Host Controller. Each UHCI Host Controller includes a root hub with two separate USB ports each, for a total of four legacy USB ports. The EHCI Host Controller includes a root hub that supports up to four USB 2.0 ports. A maximum of four USB ports are supported at any given time. The connection to either a UHCI or the EHCI is dynamic and dependent on the USB device capability, meaning that all ports support High Speed/Full Speed/Low Speed (HS/FS/LS).

3.3.5.6 AGP/ADD Connector

The evaluation board has one AGP 4X/1.5 V connector. The 855GME with 6300ESB ICH Chipset Development Kit supports AGP 2.0 specifications.

The evaluation board also provides electrical and mechanical support for AGP Digital Display (ADD) cards when using the integrated graphics capability of the 855GME. However, the BIOS which is contained in the evaluation kit does not provide support for ADD cards. Please work with your BIOS vendor to enable your specific ADD card.

Note: A jumper is required to identify whether an AGP card or ADD card is inserted. Refer to Table 10, “Jumpers and Jumper Functions” on page 38 for details.

3.3.5.7 VGA Port

The VGA port is a 15-pin DSUB female connector for output to a monitor.

3.3.5.8 LVDS Connector

The LVDS connector is used for output to a LVDS TFT panel. The Intel 855GME LVDS interface connector is based on the *Common Panel Interface Specification, Rev 1.5*.

3.3.5.9 AC'97 Audio

The evaluation board has AC'97 audio. The digital link in this development kit is AC'97 Rev 2.2 compliant.

3.3.5.10 Line Out, Line IN, CD IN, and MIC IN Connectors

The evaluation board provides Line Out, Line IN, CD IN, and MIC IN connectors.

3.3.5.11 Keyboard/Mouse Ports

There is one stacked PS/2 connector for a keyboard and mouse. The top connector is for the mouse, and the bottom connector is for the keyboard.

3.3.5.12 PCI Slot

The evaluation board has two 32-bit/33 MHz PCI connectors on the evaluation board, which supports 3.3 V and 5 V devices.

3.3.5.13 PCI-X Slot

The evaluation board has two 64-bit/66 MHz PCI-X connectors, which only supports 3.3 V devices. The PCI-X bus is capable of supporting 4 masters and has support for 64 bit addressing using DAC protocol. The PCI-X bus supports PCI 2.2 specification at 33 MHz and at PCI 64/66MHz. PCI-X 133/100 MHz is not supported. The PCI-X 66 MHz bus may support up to 533 Mbytes transfers.

3.3.5.14 Watchdog Timer (WDT)

The evaluation board contains the Watchdog Timer (WDT) feature, which provides unassisted reboot upon system hang. It also supports two modes: free running or WDT.

3.3.5.15 Serial ATA

The evaluation board includes two integrated Serial ATA devices. The SATA controllers are completely software transparent with IDE interface while providing a lower pin count and higher performance than previous standard IDE controllers.

3.3.6 Post Code Debugger

An on-board Post Code Debugger is implemented directly on the evaluation board.

3.3.7 In-Target Probe (ITP)

The evaluation board contains an in-target probe (ITP) connector for an ITPFlex. You must use an ITPFlex, which is specific to the Pentium M processor. Other ITPs will not work and if installed, could damage the platform and/or the ITP.

3.3.8 Clock Generation

The clock synthesizer on the baseboard generates and distributes the clocks used by the entire system.

3.3.8.1 System Clocks

The CK409 Clock Synthesizer is the primary source of clock generation for most of the clocks on the baseboard. The following clock groups are found on the Intel® Pentium® M Processor and Intel® 855GME Chipset Scalable Performance Board Development Kit. For more information on these clocks, see the *Intel® 855GME Chipset and Intel® 6300ESB ICH Embedded Platform Design Guide*. Table 3 presents the system clocks.

Table 3. System Clocks

Clock Name	Clock Speed
CPU	100 MHz
PCI	33 MHz
DOT	48 MHz
3V66	66 MHz
REF0	14.318 MHz
USB	48 MHz
APIC	33 MHz
SRC	100 MHz

3.3.9 Power Supply Requirements

The Intel® Pentium® M Processor, Intel® 855GME Chipset and Intel® 6300ESB ICH Development Kit must use an ATX12V power supply with a minimum of 300W support.

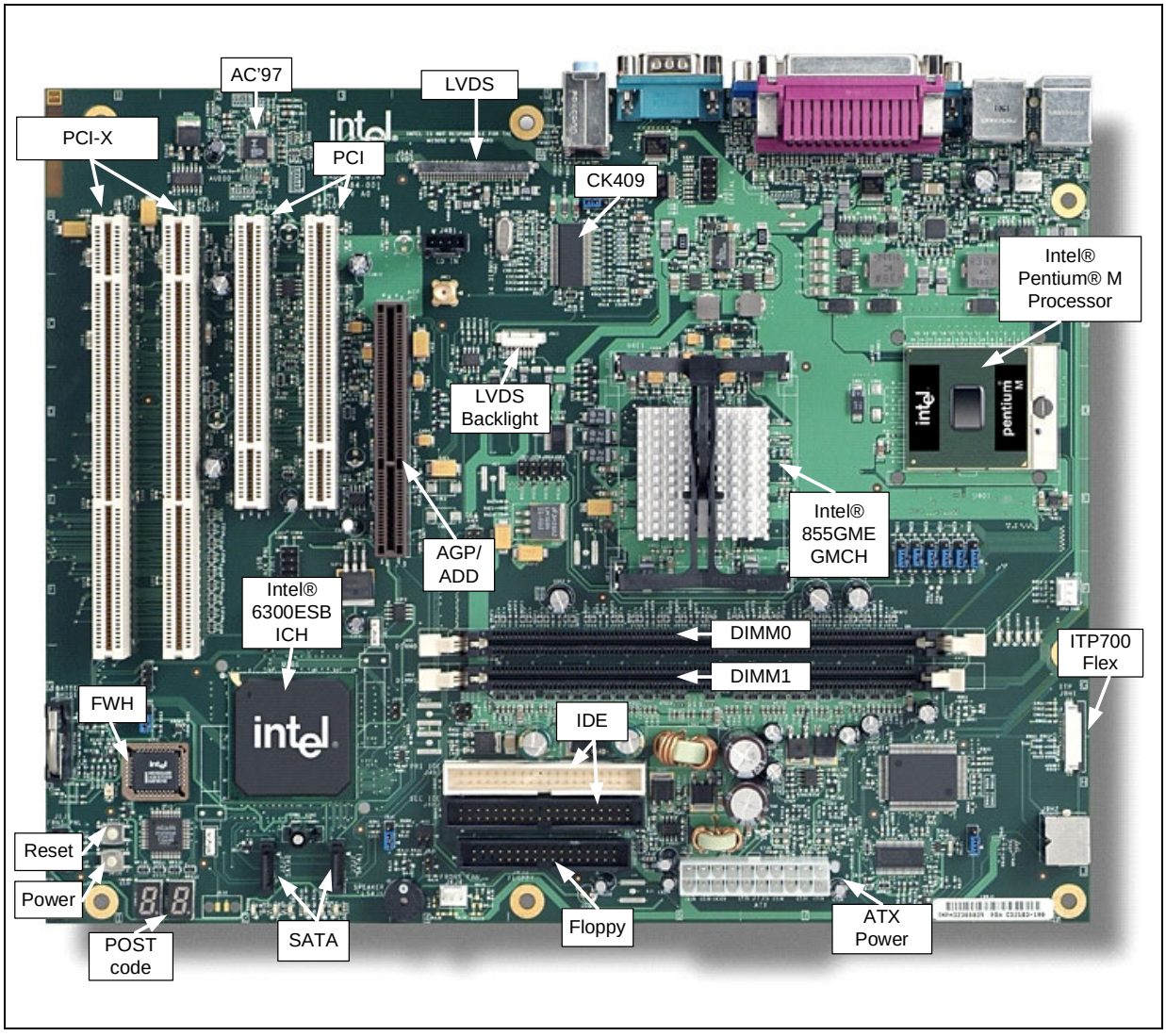
3.4 Battery Requirements

A type 2032 3 V lithium coin cell battery is included on the evaluation board.

Hardware Reference 4

This section provides reference information on the hardware, including locations of evaluation board components, connector pinout information, and jumper settings. Figure 3 shows the board layout diagram.

Figure 3. Board Layout Diagram



4.1 Chipset and Major Board Components

Table 4 presents the chipset and other major components on the evaluation board.

Table 4. Chipset and Major Board Components

Component Designator	Component Description
U6E1	Intel® 855GME Graphics Memory Controller Hub (GMCH)
U3G1	Intel® 6300ESB ICH
U8D1	Intel® Pentium® M Processor
U1H1	Intel® 82802AC Firmware Hub (FWH)

4.2 Expansion Slots and Sockets

Table 5 presents the expansion slots and sockets on the evaluation board.

Table 5. Expansion Slots and Sockets

Slot/Socket Reference Designator	Slot/Socket Description
U8D1	Processor Socket
J4C2	AGP/ADD Slot
J2B2	32/33 PCI Slot 0
J3B1	32/33 PCI Slot 1
J1B1	PCI-X Slot 0
J2B1	PCI-X Slot 1
J4G1	DDR DIMM 0
J4G2	DDR DIMM 1
U1H1	Firmware Hub (FWH) BIOS Socket
BH1G1	Battery

4.2.1 Processor Socket

There is one 478-pin µ-FCPGA processor socket on the evaluation board. The processor is keyed so that it fits into the socket in one particular orientation. The socket is released by lifting the cam lever.

Note: Do not force the processor into the socket, or you may damage the processor and/or socket. The evaluation board is designed to support future processor speeds.

4.2.2 AGP/ADD Slot Connector

Table 6 presents the pinout for AGP/ADD slot connector J4C2.

Table 6. AGP Slot Connector Pinout (Sheet 1 of 2)

Pin	B	A	Pin	B	A	Pin	B	A
1	OVRCNT#	12V	23	GND	GND	45	KEY	KEY
2	5.0V	TYPEDET#	24	3.3V AUX	Reserved	46	DEVSEL#	TRDY#
3	5.0V	Reserved	25	VCC3.3	VCC3.3	47	Vddq1.5	STOP#
4	USB+	USB-	26	AD31	AD30	48	PERR#	PME#
5	GND	GND	27	AD29	AD28	49	GND	GND

Table 6. AGP Slot Connector Pinout (Sheet 2 of 2)

Pin	B	A	Pin	B	A	Pin	B	A
6	INTB#	INTA#	28	VCC3.3	VCC3.3	50	SERR#	PAR
7	CLK	RST#	29	AD27	AD26	51	C#/BE1	AD15
8	REQ#	GNT#	30	AD25	AD24	52	Vddq1.5	Vddq1.5
9	VCC3.3	VCC3.3	31	GND	GND	53	AD14	AD13
10	ST0	ST1	32	AD_STBF1	AD_STBS1	54	AD12	AD11
11	ST2	Reserved	33	AD23	C#/BE3	55	GND	GND
12	RBF#	PIPE#	34	Vddq1.5	Vddq1.5	56	AD10	AD9
13	GND	GND	35	AD21	AD22	57	AD8	C#/BE0
14	Reserved	WBF#	36	AD19	AD20	58	Vddq1.5	Vddq1.5
15	SBA0	SBA1	37	GND	GND	59	AD_STBF0	AD_STBS0
16	VCC3.3	VCC3.3	38	AD17	AD18	60	AD7	AD6
17	SBA2	SBA3	39	C#/BE2	AD16	61	GND	GND
18	SB_STBF	SB_STBS	40	Vddq1.5	Vddq1.5	62	AD5	AD4
19	GND	GND	41	IRDY#	FRAME#	63	AD3	AD2
20	SBA4	SBA5	42	KEY	KEY	64	Vddq1.5	Vddq1.5
21	SBA6	SBA7	43	KEY	KEY	65	AD1	AD0
22	Reserved	Reserved	44	KEY	KEY	66	AGPVrefcg	AGPVrefgc

4.2.3 32-Bit PCI Slot Connector

Table 7 presents the signals assigned to the 32-bit PCI slot connectors J2B2 and J3B1.

Table 7. 32-bit PCI Slot Connector Pinout (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST#	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	TCK	A33	3.3 V	B33	C/BE2#
A3	TMS	B3	GND	A34	FRAME#	B34	GND
A4	TDI	B4	TDO	A35	GND	B35	IRDY#
A5	5 V	B5	5 V	A36	TRDY#	B36	3.3 V
A6	INTA#	B6	5 V	A37	GND	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	GND
A8	5 V	B8	INTD#	A39	3.3 V	B39	LOCK#
A9	Reserved	B9	PRSNT1#	A40	SMBCLK	B40	PERR#
A10	5 V	B10	Reserved	A41	SMBDATA	B41	3.3 V
A11	Reserved	B11	PRSNT2#	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	3.3 V
A13	GND	B13	GND	A44	AD15	B44	C/BE1#
A14	3.3 V_{AUX}	B14	Reserved	A45	3.3 V	B45	AD14

Table 7. 32-bit PCI Slot Connector Pinout (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	5 V	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	PME#	B19	5 V	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	3.3 V	B21	AD29	A52	CBE0#	B52	AD8
A22	AD28	B22	GND	A53	3.3 V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	3.3 V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	3.3 V	A56	GND	B56	AD3
A26	IDSEL	B26	C/BE3#	A57	AD2	B57	GND
A27	3.3 V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	5 V	B59	5 V
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	5 V	B61	5 V
A31	AD18	B31	3.3 V	A62	5 V	B62	5 V

4.2.4 64-Bit PCI-X Slot Connector

Table 8 presents the 64-bit 3.3 V PCI-X slot connector pinout for J1B2 and J2B1.

Table 8. 64-bit 3.3 V PCI-X Connector Pinout (Sheet 1 of 4)

Pin	Signal	Pin	Signal
A1	TRST#	B1	-12V
A2	+12V	B2	TCK
A3	TMS	B3	GND
A4	TDI	B4	TDO
A5	5V	B5	5V
A6	INTA#	B6	5V
A7	INTC#	B7	INTB#
A8	5V	B8	INTD#
A9	Reserved	B9	PRSNT1#
A10	3.3V	B10	Reserved
A11	Reserved	B11	PRSNT2#
A12	KEY	B12	KEY
A13	KEY	B13	KEY
A14	3.3V aux	B14	Reserved

Table 8. 64-bit 3.3 V PCI-X Connector Pinout (Sheet 2 of 4)

Pin	Signal	Pin	Signal
A15	RST#	B15	GND
A16	3.3V	B16	CLK
A17	GNT#	B17	GND
A18	GND	B18	REQ#
A19	PME#	B19	3.3V
A20	AD30	B20	AD31
A21	3.3V	B21	AD29
A22	AD28	B22	GND
A23	AD26	B23	AD27
A24	GND	B24	AD25
A25	AD24	B25	3.3V
A26	IDSEL	B26	C/BE3#
A27	3.3V	B27	AD23
A28	AD22	B28	GND
A29	AD20	B29	AD21
A30	GND	B30	AD19
A31	AD18	B31	3.3V
A32	AD16	B32	AD17
A33	3.3V	B33	C/BE2#
A34	FRAME#	B34	GND
A35	GND	B35	IRDY#
A36	TRDY#	B36	3.3V
A37	GND	B37	DEVSEL#
A38	STOP#	B38	PCIXCAP
A39	3.3V	B39	LOCK#
A40	SDONE	B40	PERR#
A41	SBO	B41	3.3V
A42	GND	B42	SERR#
A43	PAR	B43	3.3V
A44	AD15	B44	C/BE1#
A45	3.3V	B45	AD14
A46	AD13	B46	GND
A47	AD11	B47	AD12
A48	GND	B48	AD10
A49	AD9	B49	M66EN
A50	GND	B50	GND
A51	GND	B51	GND
A52	C/BE0#	B52	AD8

Table 8. 64-bit 3.3 V PCI-X Connector Pinout (Sheet 3 of 4)

Pin	Signal	Pin	Signal
A53	3.3V	B53	AD7
A54	AD6	B54	3.3V
A55	AD4	B55	AD5
A56	GND	B56	AD3
A57	AD2	B57	GND
A58	AD0	B58	AD1
A59	3.3V	B59	3.3V
A60	REQ64#	B60	ACK64#
A61	5V	B61	5V
A62	5V	B62	5V
A63	GND	B63	Reserved
A64	C/BE7#	B64	GND
A65	C/BE5#	B65	C/BE6#
A66	3.3V	B66	C/BE4#
A67	PAR64	B67	GND
A68	AD62	B68	AD63
A69	GND	B69	AD61
A70	AD60	B70	3.3V
A71	AD58	B71	AD59
A72	GND	B72	AD57
A73	AD56	B73	GND
A74	AD54	B74	AD55
A75	3.3V	B75	AD53
A76	AD52	B76	GND
A77	AD50	B77	AD51
A78	GND	B78	AD49
A79	AD48	B79	3.3V
A80	AD46	B80	AD47
A81	GND	B81	AD45
A82	AD44	B82	GND
A83	AD42	B83	AD43
A84	3.3V	B84	AD41
A85	AD40	B85	GND
A86	AD38	B86	AD39
A87	GND	B87	AD37
A88	AD36	B88	3.3V
A89	AD34	B89	AD35
A90	GND	B90	AD33

Table 8. 64-bit 3.3 V PCI-X Connector Pinout (Sheet 4 of 4)

Pin	Signal	Pin	Signal
A91	AD32	B91	GND
A92	Reserved	B92	Reserved
A93	GND	B93	Reserved
A94	Reserved	B94	GND

4.2.5 DDR SDRAM Slots

The evaluation board contains two DIMM slots for DDR SDRAM. Table 9 presents the DDR SDRAM slot designator and corresponding description.

Table 9. DDR SDRAM Slots

DDR SDRAM Slot Designator	DDR SDRAM Slot Description
J4G1	DIMM 0
J4J2	DIMM 1

4.2.6 Firmware Hub (FWH) BIOS Socket

The Firmware Hub (FWH), or BIOS, flash memory part fits into the 32-pin socket U1H1, giving you the option to remove and reprogram it without the use of soldering equipment. There is only one correct orientation for the FWH part to be placed into its socket. Line up the circular marking on the FWH part, denoting pin 1, with the circular marking on the evaluation board. Pin numbering proceeds clockwise around the chip from pin 1.

4.2.7 Battery

A type 2032 3 V lithium coin cell battery is used in socket BH1G1 on the evaluation board. The battery holder is beveled such that the battery fits into it in one particular orientation. The battery is held in place by a metal arm. To remove the battery, bend the arm slightly and pull the battery out.

4.3 Jumpers

The evaluation board has a number of jumpers that control various functions of the system.

Table 10 presents the descriptions of the jumpers and their settings. Default settings are recognized in bold.

Caution: There are also several two pin headers located on the evaluation board which are used for measurement of voltage planes and reference voltages. Table 11 presents the measurement headers and descriptions. **These headers should never be shorted.**

Table 10. Jumpers and Jumper Functions

Jumper	Name	Function / Comments[1]
J5E4	AGP/ADD Select	**Open**: DVO mode enabled. For use with an ADD card Short: AGP mode enabled. Must be shorted if using AGP card
J2F1	Top Swap	**Open**: Disable Top Swap mode in FWH Short: Enable Top Swap
J8J1	Enable SIO	**[1-2]**: Enable Super I/O [2-3]: Disable Super I/O
J3J1	CMOS Clear	**[1-2]**: Normal Operation [2-3]: Clear CMOS
J1G2	BIOS Config	**[1-2]**: Normal Mode [2-3]: Configuration Mode [Open]: Recovery Mode
J4J3	No Reboot	**Open**: Normal Mode Short: No Reboot
J8E1	Reserved	**Open**: Normal Short: Reserved
J5B1	Reserved	**[1-2]**: Reserved [2-3]: Normal [Open]: Reserved
J2J3	Reserved - Jumper Not Installed	**Open**: Normal Short: Reserved
J5E3	Reserved	Open: Reserved **Short**: Normal
J5E2	Reserved	Open: Reserved **Short**: Normal
J5E1	Reserved	Open: Reserved **Short**: Normal
J8F1-J8F6	VID Jumpers	**[1-2]**: Normal. [2-3]: Reserved [Open]: Reserved

1. Bolded text refers to default jumper setting.

Table 11. Measurement Headers

Header	Pin 1	Pin 2
J4G3	DIMM_VREF_1P25	Ground
J4G4	V_2P5_CORE	Ground
J4G5	HI_VREF_ICH	Ground
J4E1	HUBREF_MCH	Ground
J6C1	V_1P3_GMCH	Ground
J6C2	V_1P5_CORE	Ground

Caution: **Do not short these headers.**

4.4 On-Board Connectors

Table 12. On-Board Connectors

Connector Reference Designator	Connector Description
J7J5	ATX Power Connector
J4H2	Primary IDE Connector
J4H1	Secondary IDE Connector
J2J2	SATA 0 Connector
J3J2	SATA 1 Connector
J4J2	Floppy Connector
J9H1	Mini - ITP - 28P Connector
J9B1	Rear Chassis Fan Connector
J9F1	CPU Fan Connector
J4J4	Auxiliary Fan Connector
J5A2	LVDS Connector - 30 pin
J5C1	LVDS Panel Backlight Connector - 7pin

4.4.1 ATX Power Connectors

Table 13 presents the pinout of the ATX power connector J7J5.

Table 13. ATX Power Connector (Sheet 1 of 2)

Pin	Signal Name	Function
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	GND	Ground
4	+ 5 V	+5 V VCC
5	GND	Ground
6	+ 5 V	+5 V VCC
7	GND	Ground

Table 13. ATX Power Connector (Sheet 2 of 2)

Pin	Signal Name	Function
8	PWRGD	Power Good
9	5 VSB	Standby 5 V
10	+ 12 V	+12 V
11	3.3 V	3.3 V
12	-12 V	-12 V
13	GND	Ground
14	PS_ON#	Soft-off control
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	-5 V	-5 V
19	+5 V	+5 V VCC
20	+5 V	+5 V VCC

4.4.2 IDE Connectors

Table 14 presents the signals assigned to the IDE connector. The primary IDE connector and secondary IDE connector are J4H2 and J4H1, respectively.

Table 14. IDE Connector Pinout (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	Reset IDE	21	PDDREQ
2	Ground	22	Ground
3	Host Data 7	23	I/O Write#
4	Host Data 8	24	Ground
5	Host Data 6	25	I/O Read#
6	Host Data 9	26	Ground
7	Host Data 5	27	IOCHRDY
8	Host Data 10	28	Ground
9	Host Data 4	29	PDDACK
10	Host Data 11	30	Ground
11	Host Data 3	31	IRQ14
12	Host Data 12	32	Reserved
13	Host Data 2	33	Addr1
14	Host Data 13	34	Primary IDE Cable Detect
15	Host Data 1	35	Addr 0
16	Host Data 14	36	Addr 2
17	Host Data 0	37	Chip Select 0#

Table 14. IDE Connector Pinout (Sheet 2 of 2)

Pin	Signal	Pin	Signal
18	Host Data 15	38	Chip Select 1#
19	Reserved	39	Activity
20	Key	40	Ground

4.4.3 SATA Connectors

Table 15 presents the signals assigned to the SATA connectors J2J2 and J3J2.

Table 15. SATA Connector Pinout

Pin	Signal
1	GND
2	A+
3	A-
4	GND
5	B-
6	B+
7	GND

4.4.4 Floppy Drive Connector

Table 16 presents the signals assigned to the floppy drive connector, J4J2.

Table 16. Floppy Drive Connector Pinout

Pin	Signal	Pin	Signal
1	Ground	2	Drive Enable 0
3	Ground	4	Reserved
5	Key	6	Drive Enable 1
7	Ground	8	Index
9	Ground	10	Motor Enable A#
11	Ground	12	Reserved
13	Ground	14	Drive Select A#
15	Ground	16	Reserved
17	Reserved	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	Reserved	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

4.4.5 ITP700FLEX Connector

See Section 3.3.7 and ITP documentation for information on the In-Target Probe (ITP). See *ITP700 Debug Port Design Guide* (http://www.intel.com/design/Xeon/guides/249679.htm).

4.4.6 Fan Connectors

There are three 12 V fan connectors on the evaluation board. Use connector J9F1 for the CPU fansink. If you choose to install another 12 V fan or fansink on your evaluation board, you can use the two auxiliary fan connectors J9B1 and J4J4.

4.4.7 LVDS Connectors

Table 17 presents the pinout of the LVDS panel connector J5A2. Table 18 presents the pinout of the LVDS panel backlight connector J5C1.

Table 17. LVDS Panel Connector Pinout

Pin	Signal
1	Ground
2	3.3 V (Data Power)
3	3.3 V (Data Power)
4	3.3 V (Control Power)
5	Reserved
6	DDCPCLK
7	DDCPDATA
8	YAM(0)
9	YAP(0)
10	Ground
11	YAM(1)
12	YAP(1)
13	Ground
14	YAM(2)
15	YAP(2)
16	Ground
17	CLKAM
18	CLKAP
19	Ground
20	YBM(0)
21	YBP(0)
22	Ground
23	YBM(1)
24	YBP(1)
25	Ground
26	YBM(2)
27	YBP(2)
28	Ground
29	CLKBM
30	CLKBP

Table 18. LVDS Panel Backlight Connector Pinout (Sheet 1 of 2)

Pin	Signal
1	+12 V (Backlight Power)
2	Ground
3	Ground

Table 18. LVDS Panel Backlight Connector Pinout (Sheet 2 of 2)

Pin	Signal
4	+5 V (Inverter Control Power)
5	SMB_CLK
6	SMB_DATA
7	BKLTEN (Backlight Enable)

4.5 On-Board Headers

Table 19. On-Board Headers

Header Reference Designator	Header Description
J4J1	Intruder Header
J3E1	USB Front/Back Panel Header
J4B1	CD IN Header
J6B1	Serial Port Header
J1J1	Front Panel Header
J1J2	Infrared Header

4.5.1 Intruder Header

The Intruder header, J4J1, is a 2 pin jumper which can be attached to a switch that is activated by the system's case being opened.

4.5.2 USB Front Panel Header

Table 20 presents the pinout of the USB front panel header, J3E1.

Table 20. USB Front Panel Header

Pin	Signal	Pin	Signal
1	5 V (fused)	2	5 V (fused)
3	USBP2#	4	USBP3#
5	USBP2	6	USBP3
7	Ground	8	Ground
9	Key	10	Reserved

4.5.3 CD IN Header

Table 21 presents the pinout of the CD IN header, J4B1.

Table 21. CD IN Header

Pin	Signal
1	LCD
2	CDGND
3	CDGND
4	RCD

4.5.4 Serial Port Header

Table 22 presents the pinout of the Serial Port header, J6B1.

Table 22. Serial Port Header

Pin	Signal	Pin	Signal
1	DCD	2	Serial In (SIN)
3	Serial Out (SOUT)	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	Key

4.5.5 Front Panel Header

Table 23 presents the pinout of the Front panel header, J1J1.

Table 23. Front Panel Header

Pin	Signal	Pin	Signal
1	HD_LED	2	FP_PWR/SLP
3	HD_LED_N	4	FP PWR/SLP
5	GND	6	PWR_SW_P
7	RST_SW_P	8	GND
9	Reserved	10	No Pin

4.5.6 Infrared Header

Table 23 presents the pinout of the Infrared header, J1J2.

Table 24. Infrared Header

Pin	Signal	Pin	Signal
1	Reserved	2	Key
3	+5 V	4	Ground
5	IRTX	6	IRRX

4.6 Buttons

The evaluation board has power and reset buttons. Table 25 presents the switch reference designation and corresponding button description.

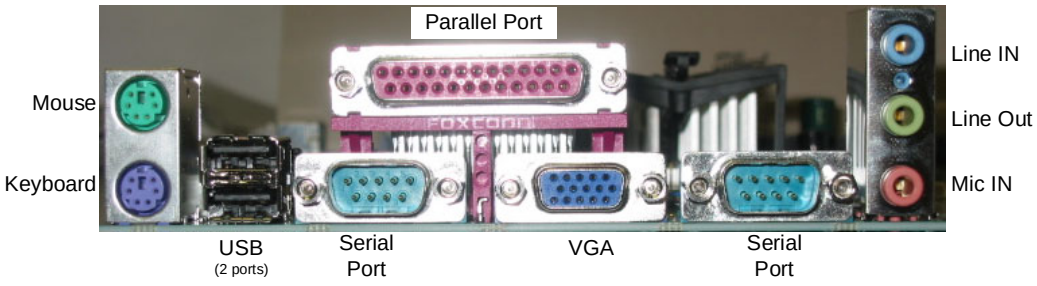
Table 25. Buttons

Switch Reference Designator	Switch Description
SW1J1	Power Button
SW1H1	Reset Button

4.7 Peripheral Connectors

The evaluation board contains a number of connectors for external system devices and peripherals. Figure 4 shows the peripheral connectors.

Figure 4. Peripheral Connectors



4.7.1 Dual Stacked USB Connector

Table 26 presents the signals assigned to the dual stacked USB connector.

Table 26. USB Connector Pinout

Pin	Signal
1,5	Power (fused)
2,6	USBP1# [USBP0#]
3,7	USBP1 [USBP0]
4,8	Ground

4.7.2 PS/2-Style Mouse and Keyboard Connectors

Table 27 presents the signals assigned to the PS/2-style keyboard and mouse connectors. The keyboard port is on the bottom, and the mouse port is on the top.

Table 27. PS/2-Style Mouse and Keyboard Pinout

Pin	Signal
1, 7	Data
2,8	Reserved
3,9	Ground
4,10	+5 V (fused)
5,11	Clock
6,12	Reserved

4.7.3 VGA Port

Table 28 presents the signals assigned to the VGA port.

Table 28. VGA Port Signals

Pin	Signal
1	Red
2	Green
3	Blue
4	Reserved
5	Ground
6	Analog Ground
7	Analog Ground
8	Analog Ground
9	V_{CC}
10	Ground
11	Reserved
12	DDC Data
13	Horizontal Sync
14	Vertical Sync
15	DDC Clock

4.7.4 Parallel Port

Table 29 presents the signals assigned to the parallel port connector.

Table 29. Parallel Port Connector Pinout

Pin	Signal	Pin	Signal
1	Strobe#	14	Auto Feed#
2	Data Bit 0	15	Fault#
3	Data Bit 1	16	INIT#
4	Data Bit 2	17	SLC IN#
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Paper end	25	Ground
13	SLCT		

4.7.5 Serial Ports

Table 30 presents the signals assigned to the serial port connector.

Table 30. Serial Port Connector Pinout

Pin	Signal
1	DCD
2	Serial In (SIN)
3	Serial Out (SOUT)
4	DTR
5	Ground
6	DSR
7	RTS
8	CTS
9	RI

4.8 Voltage Identification for the Intel® Pentium® M Processor

There are six voltage identification pins on the Pentium M processor. These signals may be used to support automatic selection of V_{CC_CORE} voltages and are needed to cleanly support voltage specification variations on current and future processors. VID[5:0] is defined in Table 31.

Table 31. VID vs. V_{CC_CORE} Voltage (Sheet 1 of 2)

VID						V_{CC_CORE}	VID						V_{CC_CORE}
5	4	3	2	1	0	V	5	4	3	2	1	0	V
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748

Table 31. VID vs. V_{CC_CORE} Voltage (Sheet 2 of 2)

VID						V_{CC_CORE}	VID						V_{CC_CORE}
5	4	3	2	1	0	V	5	4	3	2	1	0	V
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

BIOS Overview 5

The Intel® 855GME BIOS was created using AMIBIOS8* technology created by AMI*.

The following documents are available to overview the high-level features of AMIBIOS8:

- Amibios8.pdf
- AMIBIO8Brochure.pdf
- AboutAMIBIOS8.pdf

These files, and others, are also available for download from AMI's website (http://www.ami.com).

5.1 Power-On and Configuration

5.1.1 Power On

Upon power-on, the Intel® 855GME BIOS will initialize the board hardware and peripherals, communicating its progress by writing status codes to an I/O port (80h). These status codes may be monitored with the on board POST code debugger.

Documentation on the status codes sent to port 80h is available in the file AMIBIOS-codes.pdf. This file can be downloaded from AMI's website (http://www.ami.com).

After most of the hardware has been configured, including video (whether it be on-board or PCI), the user is presented with a splash screen. This splash screen displays the following information:

- BIOS information, such as build time and version
- CPU configuration
  - — Number of CPUs in the system
  - — Speed of the CPUs
  - — Brand string
  - — Family/Model/Stepping
  - — Microcode update loaded

All of memory is then tested, and the progress of the test is displayed on the screen. This memory test may be skipped by pressing the <ESC> key at any time during the test.

Following the memory test, IDE devices are detected. If CMOS memory has been corrupted or is otherwise invalid, you will be prompted to load default CMOS data and continue or enter the setup utility. Press <F1> to enter the setup utility or press <F2> to load default values into CMOS and continue.

After the IDE devices are displayed, the current hardware configuration is shown, and the boot device is chosen. Then control is handed over to the boot loader on the selected boot device.

5.1.2 BIOS Setup Configuration

The Intel 855GME BIOS provides a setup utility to customize your board. At any point during the display of the first splash screen, pressing the <DEL> key will enter BIOS setup.

The BIOS Setup utility has been functionally divided into five sections to categorize the setup options:

- Main
- Advanced
- PCI/PNP (not discussed here)
- Boot
- Security (not discussed here)
- Chipset
- Exit

These sections can be navigated using all four arrow keys. The <UP> and <DOWN> keys toggle between setup options in any given section. The <LEFT> and <RIGHT> keys switch between main BIOS setup sections. Each of these sections will be discussed briefly, in turn.

5.1.3 Help on Options

It should be noted that not all setup options are documented in this guide. The setup utility in the BIOS contains brief help descriptions for almost every setup option available. When any given setup option is highlighted (selected by moving the cursor to the item with the arrow keys), a brief description of that option is displayed in a pane on the right-hand side of the screen.

5.1.4 Main Setup

The Main BIOS setup screen contains mostly informative information on the BIOS. The following information is displayed:

- BIOS version
- BIOS build date
- BIOS ID

Please use this information when engaging with Intel customer support.

5.1.4.1 Time and Date

The Main Setup section contains fields to control the date and the time of the system. These should be set the first time the setup utility is entered.

5.1.5 Advanced Setup

The Advanced BIOS setup screen contains various menu items that allow you to configure the following system components:

- CPU
- IDE (not discussed here)
- Floppy (not discussed here)
- ACPI (not discussed here)
- Event Log (not discussed here)
- Super I/O (not discussed here)
- USB (not discussed here)
- Onboard Devices

5.1.5.1 CPU Configuration

CPU Frequency Multiplier

The Intel 855GME board adaptation allows for the user to set the operating frequency of the processors in the system. The CPU Frequency Multiplier field accepts a decimal number representing the processor's internal clock multiplier ratio. The following equation defines how this field affects processor operating frequency:

Processor Frequency = (CPU Frequency Multiplier) * (FSB Frequency) / 4

For example, a CPU Frequency Multiplier value of "20" on a board that is populated with 400 MHz FSB processors will result in an effective processor operating frequency of 2.0 GHz.

It should be noted that not all multipliers are allowable. While the setup option may allow a value to be entered, it is not guaranteed that the entered multiplier will actually result in the intended processor frequency. The effective frequency of the processor depends on the supported frequency range of the processor. If a value entered in this option is not explicitly supported by the processor, the system should exhibit the following behavior:

- If the multiplier would target a processor frequency of below 1.2 GHz, the system will strap to 800 MHz
- If the multiplier would target a processor frequency between 1.2 GHz and the lowest supported processor frequency, the system will strap to the lowest supported processor frequency.
- If the multiplier would target a processor frequency above the highest supported processor frequency, the system will strap to the highest supported processor frequency.

5.1.6 Boot Setup

The Boot Setup section contains options that controls boot devices, boot order, and other aspects of the boot process. Most of these options will not be documented here.

Quick Boot

The Quick Boot option determines whether or not a complete memory test is performed by the BIOS during boot. Enabling this option will speed up boot time of large memory configurations greatly. It is disabled by default.

5.1.7 Chipset Setup

This setup section contains options that allow the user to configure various parameters that are specific to the chipset silicon present on the board. The following silicon is configurable through this setup section:

- 855GME chipset
- 6300ESB ICH

5.1.8 Exit

After BIOS setup modifications have been done, you have several choices for leaving the setup utility, which are displayed on the Exit Setup screen.

- Save and Exit (F10)
- No Save and Exit
- Discard Changes (F7)
- Load Optimal Defaults (F8)
- Load Failsafe Defaults (F9)

5.1.8.1 Save Changes and Exit

This option can be chosen to save all changes made to CMOS configuration since entering BIOS setup utility and rebooting the system. All changes made in the setup utility will take affect on the subsequent boot.

5.1.8.2 Discard Changes and Exit

This option can be chosen to exit the setup utility without saving any CMOS configuration changes that have been made. Choosing this option will allow the boot to continue from where it left off before entering the setup utility.

5.1.8.3 Discard Changes

If you have made changes that you wish to undo, this option can be used to restore the CMOS buffer to the same state it was in at setup utility entry.

5.1.8.4 Load Optimal/Failsafe Defaults

Both of these options load a pre-programmed set of configuration data to CMOS.

5.1.8.5 Shortcuts

In addition to using the Exit Setup screen to choose your method of leaving the setup utility, you can also use function keys (noted above) from any point inside the setup utility.

5.2 Updating the BIOS

AMI provides an MS-DOS utility that may be used to replace the BIOS on your 855GME board with a newer version. The utility may be invoked via MS-DOS command line with one parameter, being the .rom file that represents the new BIOS image. The .rom file may be located in any location in the system accessible from MS-DOS.

This utility, along with instructions, is available for download from AMI's website (http://www.ami.com). Although the name of the actual executable file changes from release to release, this tool is packaged under the name AMIFLASH.

5.3 Troubleshooting

5.3.1 Error Messages

In some situations, you may be faced with error messages from the BIOS. AMIBIOS-Error-Messages.pdf describes some of the messages you may see. This document, along with others, is available online from AMI's website (http://www.ami.com).

5.3.2 Status Codes

During the boot process, the 855GME BIOS communicates its progress to the user by writing status codes to an I/O port (80h). These status codes may be monitored by installing a POST diagnostic card in the short debug PCI slot.

Documentation on the status codes that are sent to port 80h is in the file AMIBIOS-codes.pdf which is available for download from AMI's website (http://www.ami.com).

5.3.3 Fatal Error Codes

Some memory configurations may cause the system to stop because the BIOS can no longer function. These conditions are specific to the 855GME board adaptation, and are not documented with the reset of the POST codes in the AMI documentation. Table 32 details the possible board-specific fatal error codes that may be observed.

Table 32. Board-Specific Fatal Error Codes

Post Code	Name	Description
E1	Memory Not Present	Make sure memory is populated in the system. If memory has been populated in the system, it is possible that the BIOS to skipped DIMMs that are not valid for the current board configuration, and had no valid DIMMs to initialize.
E2	Memory Type Mismatch	Memory has been placed in the system that is not Registered ECC x72 DDR. Check all DIMMs.
E3	Memory Width Error	The silicon on the board doesn't support the DRAM width of one of the DIMMs populated on the board. Check the width of all DIMMs and replace any non-supported DIMMs.
E4	Memory Channel Mismatch	At least one DIMM pair (channel A and channel B) do not match, or only one DIMM is populated in the socket pair.
EA	Memory Timing Error	At least one DIMM has been placed in the system that is not fast enough to run in the current configuration. Inspect and replace slow DIMMs.
EE	Memory Size Not Supported	The size of at least one DIMM is not supported by the BIOS. Inspect and replace any unsupported DIMMs.
EF	DIMM Population Order Error	Mixed single-rank and double-rank DIMMs have been populated in the wrong order. Reorder the DIMMs such that any of the double-rank DIMMs are farther from the MCH than any of the single-rank DIMMs.

Note: The BIOS contained on your board may not generate all of the error codes listed above.

Schematics A

This section provides the schematics for the Intel® Pentium® M Processor, Intel® 855GME Chipset and Intel® 6300ESB ICH Development Kit.

To obtain the latest version of the bill of materials, contact your local Intel representative.

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE

PAGE #	COMENT/FUNCTION
1	COVER PAGE.
2	TABLES: BLOCK DIAGRAM
3	CORE: CK_409 (MAIN CLOCK GENERATOR)
4	CORE: CPU SOCKET 1 OF 2
5	CORE: CPU SOCKET 2 OF 2
6	CORE: CPU: PULL-UPS, TJPRO CONN
7	CORE: GMCH: DDR, HOST, HI INTERFACES
8	CORE: GMCH VIDEO AND MISC INTERFACES
9	CORE: GMCH POWER AND GND
10	CORE: GMCH CIRCUITRY
11	CORE: GMCH PLL, STRAPS & MISC CLOCK DRIVERS
12	CORE: DDR SERIES TERMINATION
13	CORE: DIMM CONNECTORS
14	CORE: DDR PARALLEL TERM (STROBES, CNTL)
15	CORE: DDR VTERM CAPS
16	CORE: AGP DIGITAL DISPLAY CONNECTOR
17	CORE: VGA CONNECTOR
18-19	CORE: LVDS CONNECTOR
20	ICH: PCI & IDE INTERFACES
21	ICH: CPU, PM, SATA, USB & HI INTERFACES
22	ICH: PCI-X, AUDIO & SERIAL PORT INTERFACES
23	ICH: ICH PULL-UP/PULL-DOWNS, BATTERY
25	ICH: IDE PRIMARY & SECONDARY
26	ICH: USB BACK PANEL CONNECTORS AND POWER
27	ICH: USB FRONT PANEL CONNECTOR AND POWER
28	ICH: PCI SLOTS 2 - 1
29	ICH: PCI TERMINATION
30	ICH: PCI-X SLOTS 2 - 1
31	ICH: PCI-X TERMINATION
32-33	ICH: SMBUS ISOLATION
34	ICH: SERIAL ATA CONNECTORS
35-36	AUDIO: CODEC
37	AUDIO: CD-IN, LINE-IN
38	AUDIO: MIC-IN, LINE-OUT
39	AUDIO: VREG
40	SIO: LPC47M102
41	SIO: FLOPPY
42	SIO: KEYBOARD & MOUSE PORTS (PS/2)
43	SIO: PARALLEL PORT
44	SIO: COM1-COM3
45	FWH: MFG MODE AND RECOVERY JUMPERS

PAGE #	COMPONENT/FUNCTION
46	GLUE4
47	PC SPEAKER
48	FRONT PANEL HEADER
49	LABELS / MOUNTING HOLES
50	FAN: FAN HEADERS (3)
51	VREG: 2.5V MEMORY, STANDBY-MEMORY
52	VREG: 1.25V MEMORY VTT
53	VREG: ATX POWER CONNECTOR 2X10
54	VREG: PCI VAUX, USB_NCH & USB_PCH
55	VREG: 1.5V STBY & 3.3V STBY
56	VREG: BULK DECOUPLING
57	VREG: 2.5V STR DECOUPLING
58	VREG: CORE 1.5V & 1.8V
59	VREG: CPU MAIN REGULATOR (CPU_CORE)
60	VREG: CPU DECOUPLING, CPU VREG DECOUPLING
61	VREG: GMCH CORE REGULATOR & VCCP REGULATOR
62	DEBUG: TITLE PAGE
63	DEBUG: ITP PORT AND PULL-UPS
64	DEBUG: CPU STATUS LEDS
65	DEBUG: SYSTEM LEDS, PWR & RESET BUTTONS
66	DEBUG: PORT 80 DECODER
67	DEBUG: VID JUMPERS, SMBUS HEADER, HUBLINK PROBE
68	DEBUG: SMA CONNECTORS, SMI/STPCLK INJECTION
69	REVISION HISTORY

855GMEFB

FAB C
REV 3

PBA: C32583-301
PB: C32584-003

POWER SYMBOLS USED:

VCC3
VCC
VCCP
+12V
-12V

NOTES:

3. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.
4. VCCP = +1.05 VOLTS UNLESS OTHERWISE SPECIFIED.

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

DRAWING
855GMEFB.SCH_1.1
Wed Apr 13 15:39:22 2005

INTEL(R) PENTIUM(R) M PROCESSOR
INTEL(R) 82855GME GMCH
INTEL(R) FWE6300ESB I/O CONTRLR HUB

BOM RELEASE DATE		PB NUMBER C32583-301			
SIGNATURE	DATE	intel	5000 W. CHANDLER BLVD CHANDLER, AZ 85044		
DRN BY		TITLE SCH, PBA, 855GMEFB			
CHK BY					
ENGR APVD					
APVD					
APVD		INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 1/69	REV C3

~TO ENABLE AGP ADD A JUMPER ACCROSS J5E4 (PAGE 11)

UPGA478 SOCKET

PSB

CK_409 CLOCK (SEE PG 4 FOR CLOCK MAP)

SM BUS

ICS91718

ADD CONN DVO B & C OR AGP 4X~

LVDS CONN

DAC

BACKLIGHT CONNECTOR

SM BUS

855GME GMCH

SM BUS

DOUBLE DATA RATE SDRAM

(2-DDR SDRAM DIMMS)

DIMM 0:1

HUB INTERFACE

SM BUS

PCI (33MHZ)

PCI SLOTS 1

PCI SLOTS 2

IDE CONN PRI & SEC

SERIAL ATA PORT 0

PORT 1

6300ESB: I/O CONTROLLER HUB

PCI-X (66MHZ)

PCI-X SLOTS 1

PCI-X SLOTS 2

BACK PANEL USB PORT 0

USB PORT 1

AC LINK

SERIAL PORT 1

SERIAL PORT 2

LPC BUS

FRONT PANEL USB PORT 2

USB PORT 3

PORT80

SMSC I/O

FWH: FIRMWARE HUB

AC '97 AUDIO CODEC REV 2.2

AMP

STEREO LINE OUT

STEREO LINE OUT

MIC IN

AUX CD/AUDIO IN

STEREO LINE IN

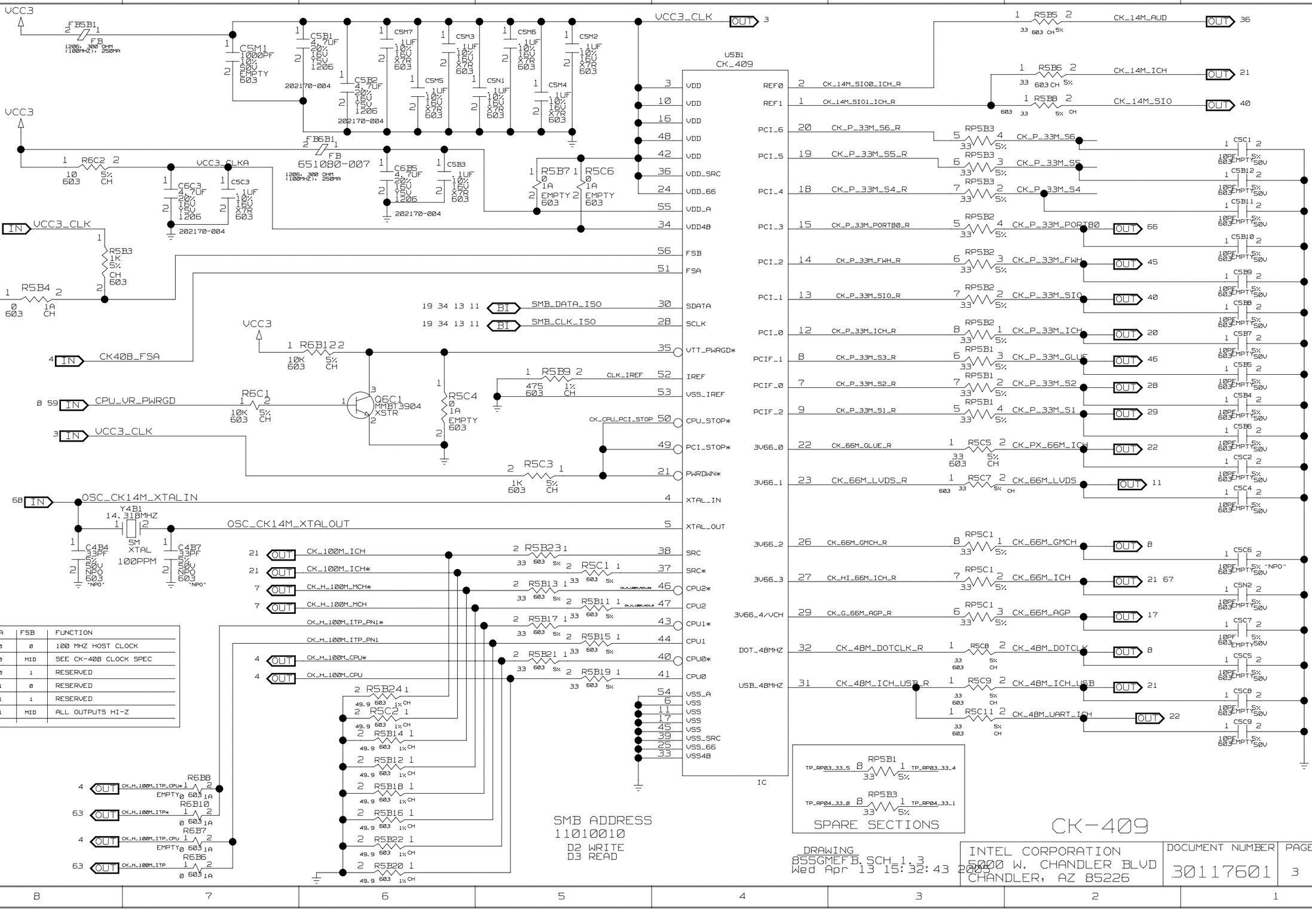
PS2 MOUSE & KEYBOARD

PARALLEL (1) SERIAL (1)

FLOPPY DISK DRIVE CONN

[BLOCK DIAGRAM]

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.2 Wed Apr 13 15:32:41 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	2	C3


U5B1
CK_409
VCC3_CLK
OUT 3
VDD 3
VDD 10
VDD 16
VDD 48
VDD 42
VDD_SRC 36
VDD_66 24
VDD_A 55
VDD48 34
FSB 56
FSA 51
SDATA 30
SCLK 28
VTT_PWRGD* 35
IREF 52
VSS_IREF 53
CPU_STOP* 50
PCI_STOP* 49
PWRDWN* 21
XTAL_IN 4
XTAL_OUT 5
SRC 38
SRC* 37
CPU2* 46
CPU2 47
CPU1* 43
CPU1 44
CPU0* 40
CPU0 41
VSS_A 54
VSS 6
VSS 11
VSS 17
VSS 45
VSS_SRC 39
VSS_66 25
VSS48 33
IC
REF0 2 CK_14M_SIO0_ICH_R
REF1 1 CK_14M_SIO1_ICH_R
PCI_6 20 CK_P_33M_S6_R
PCI_5 19 CK_P_33M_S5_R
PCI_4 18 CK_P_33M_S4_R
PCI_3 15 CK_P_33M_PORTB0_R
PCI_2 14 CK_P_33M_FWH_R
PCI_1 13 CK_P_33M_SIO_R
PCI_0 12 CK_P_33M_ICH_R
PCIF_1 8 CK_P_33M_S3_R
PCIF_0 7 CK_P_33M_S2_R
PCIF_2 9 CK_P_33M_S1_R
3V66_0 22 CK_66M_GLUE_R
3V66_1 23 CK_66M_LVDS_R
3V66_2 26 CK_66M_GMCH_R
3V66_3 27 CK_HI_66M_ICH_R
3V66_4/VCH 29 CK_G_66M_AGP_R
DOT_48MHZ 32 CK_48M_DOTCLK_R
USB_48MHZ 31 CK_48M_ICH_USB_R
R5B5 CK_14M_AUD OUT 36
R5B6 CK_14M_ICH OUT 21
R5B8 CK_14M_SIO OUT 40
RP5B3 CK_P_33M_S6 OUT 20
RP5B3 CK_P_33M_S5 OUT 46
RP5B3 CK_P_33M_S4 OUT 28
RP5B2 CK_P_33M_PORTB0 OUT 66
RP5B2 CK_P_33M_FWH OUT 45
RP5B2 CK_P_33M_SIO OUT 40
RP5B2 CK_P_33M_ICH OUT 20
RP5B1 CK_P_33M_GLUE OUT 46
RP5B1 CK_P_33M_S2 OUT 28
RP5B1 CK_P_33M_S1 OUT 29
R5C5 CK_PX_66M_ICH OUT 22
R5C7 CK_66M_LVDS OUT 11
RP5C1 CK_66M_GMCH OUT 8
RP5C1 CK_66M_ICH OUT 21 67
RP5C1 CK_66M_AGP OUT 17
R5C8 CK_48M_DOTCLK OUT 8
R5C9 CK_48M_ICH_USB OUT 21
R5C11 CK_48M_UART_ICH OUT 22
C5C1 C5B12 C5B11 C5B10 C5B9 C5B8 C5B7 C5B5 C5B4 C5B6 C5C2 C5C4 C5C6 C5N2 C5C7 C5C5 C5C8 C5C9
10PF 603 EMPTY 5% 50V
C5C6 5% "NPO"
IN 3 VCC3_CLK
R5B3 1K 5% CH 603
R5B4 0 603 1A CH
IN 4 CK408_FSA
R6B122 10K 603 5% CH
IN 8 59 CPU_VR_PWRGD
R6C1 10K 603 5% CH
Q6C1 MMBT3904 XSTR
R5C4 0 1A EMPTY 603
IN 3 VCC3_CLK
R5C3 1K 603 5% CH
IN 68 OSC_CK14M_XTALIN
OSC_CK14M_XTALOUT
Y4B1 14.318MHZ SM XTAL 100PPM
C4B4 C4B7 33PF 50V 5% NPO 0603 "NPO"
VCC3_CLKA
R6C2 10 603 5% CH
C6C3 4.7UF 20% 16V Y5V 1206
C5C3 .1UF 10% 16V X7R 603
202170-004
FB B5B1 FB 1206, 300 OHM (100MHZ), 250MA
FB B6B1 FB 651080-007 1206, 300 OHM (100MHZ), 250MA
C5B1 4.7UF 20% 16V Y5V 1206
C5M1 1000PF 10% 50V EMPTY 603
C5B2 4.7UF 20% 16V Y5V 1206
C5M7 C5M3 C5M6 C5M2 C5M5 C5N1 C5M4 .1UF 10% 16V X7R 603
C6B5 4.7UF 20% 16V Y5V 1206
C5B3 .1UF 10% 16V X7R 603
R5B7 0 1A EMPTY 603
R5C6 0 1A EMPTY 603
19 34 13 11 BI SMB_DATA_ISO
19 34 13 11 BI SMB_CLK_ISO
CLK_IREF
CK_CPU_PCI_STOP
CK_100M_ICH OUT 21
CK_100M_ICH* OUT 21
CK_H_100M_MCH* OUT 7
CK_H_100M_MCH OUT 7
CK_H_100M_ITP_PN1*
CK_H_100M_ITP_PN1
CK_H_100M_CPU* OUT 4
CK_H_100M_CPU OUT 4
R5B23 R5C1 R5B13 R5B11 R5B17 R5B15 R5B21 R5B19 33 603 5%
R5B24 R5C2 R5B14 R5B12 R5B18 R5B16 R5B22 R5B20 49.9 603 1% CH
R6B8 R6B10 R6B7 R6B6 0 603 1A EMPTY
CK_H_100M_ITP_CPU* OUT 4
CK_H_100M_ITP* OUT 63
CK_H_100M_ITP_CPU OUT 4
CK_H_100M_ITP OUT 63
FSA FSB FUNCTION
0 0 100 MHZ HOST CLOCK
0 MID SEE CK-408 CLOCK SPEC
0 1 RESERVED
1 0 RESERVED
1 1 RESERVED
1 MID ALL OUTPUTS HI-Z
SMB ADDRESS
11010010
D2 WRITE
D3 READ
RP5B1 TP_RP03_33_5 TP_RP03_33_4
RP5B3 TP_RP04_33_8 TP_RP04_33_1
33 5%
SPARE SECTIONS
CK-409
DRAWING
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5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
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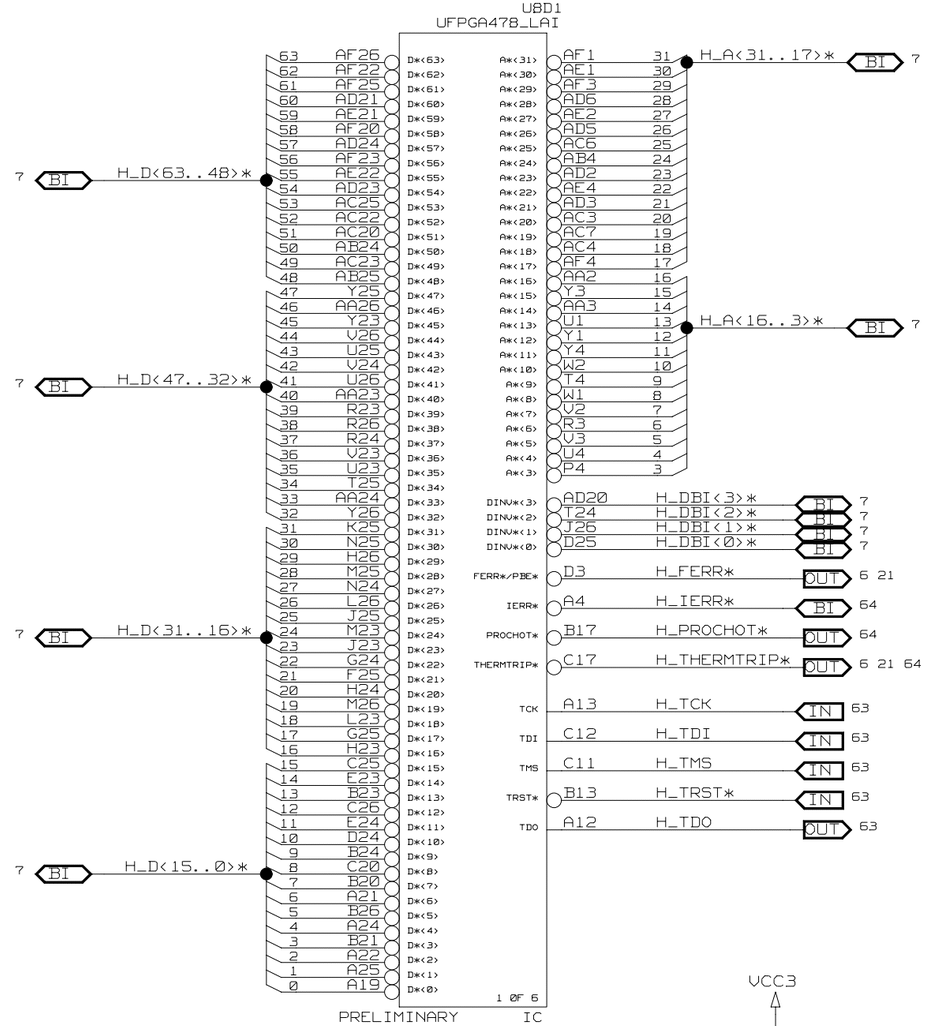

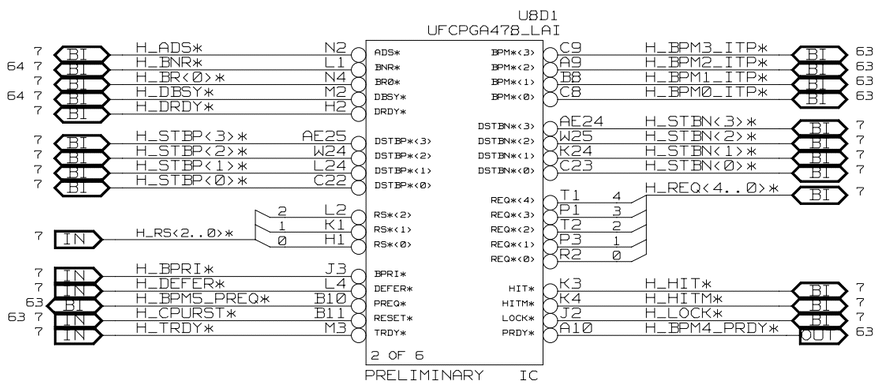

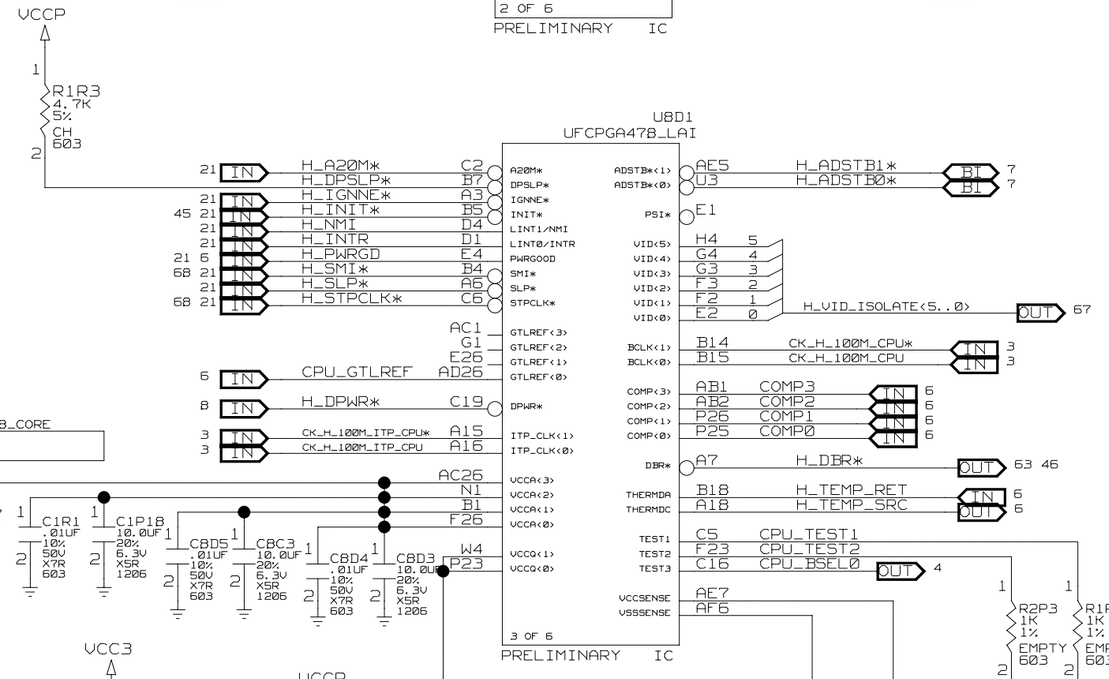

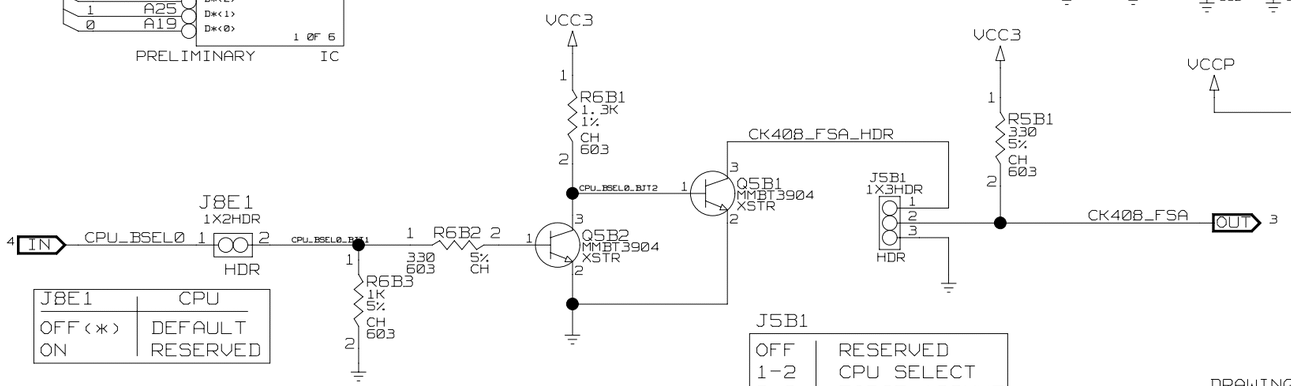

J8E1	CPU
OFF(*)	DEFAULT
ON	RESERVED

J5B1	
OFF	RESERVED
1-2	CPU SELECT
2-3	FORCE 100MHZ

CPU 1 OF 2

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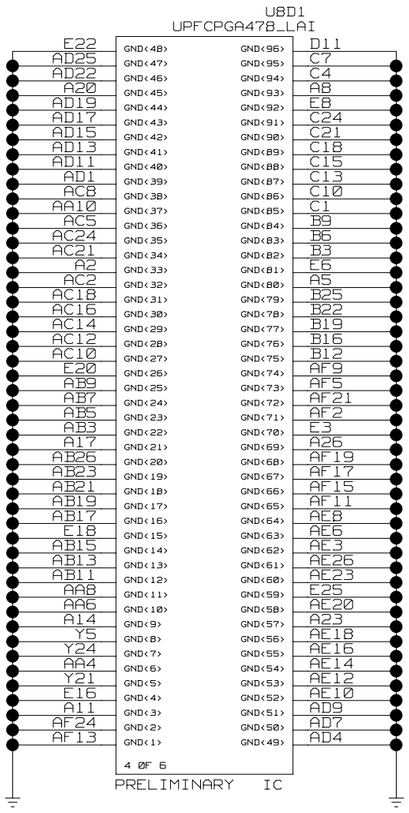

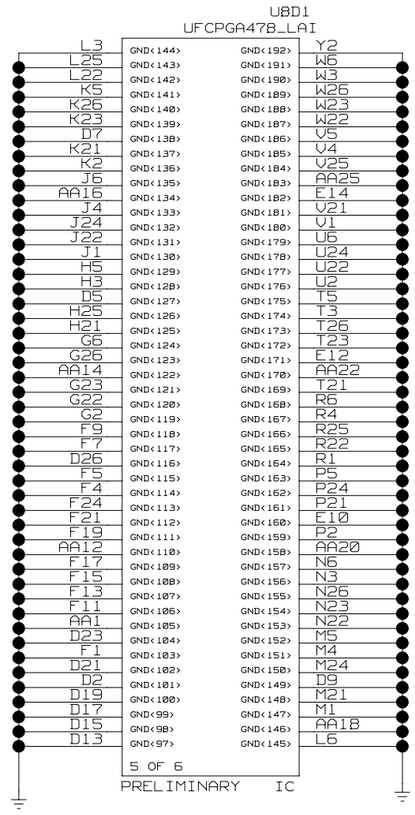

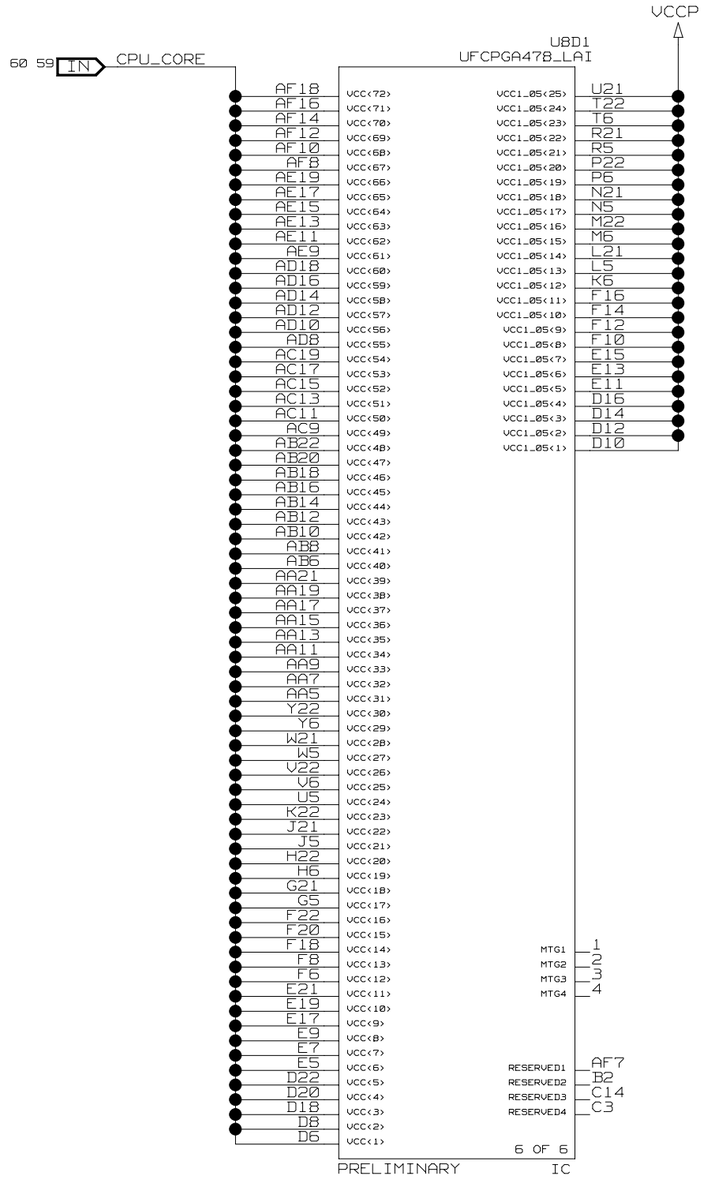

CPU 2 OF 2

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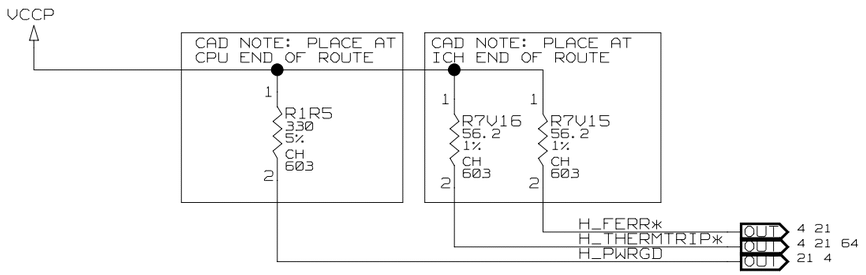
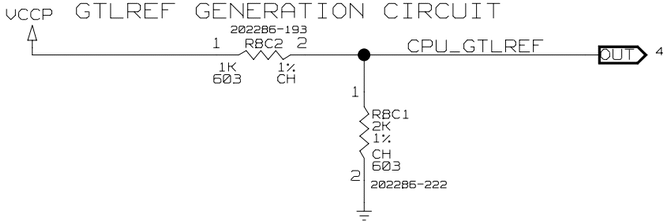
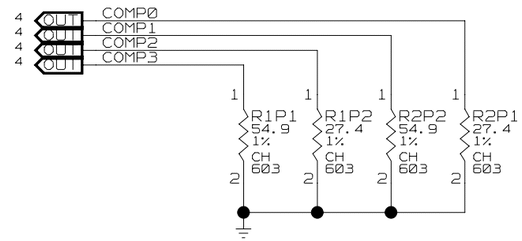
CPU SIGNAL TERMINATION



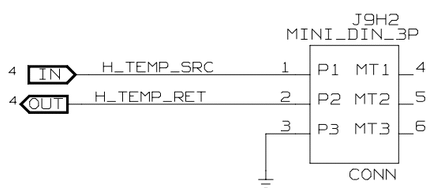
VCCP GTLREF GENERATION CIRCUIT



CPU COMP RESISTORS



MINIDIN3 FOR CPU THERMAL DIODE MONITORING



CPU CIRCUITS

DRAWING				
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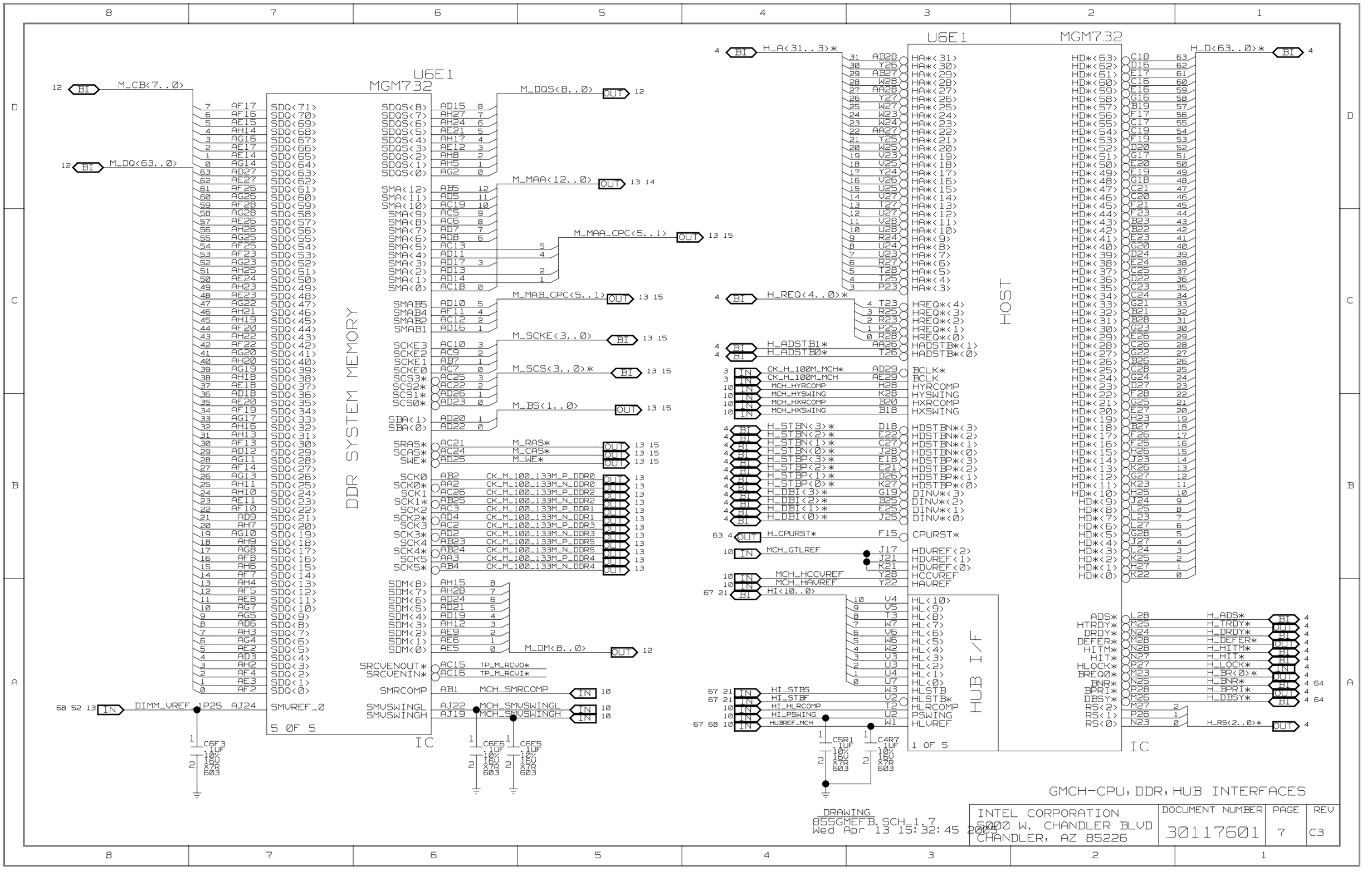
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SCK4
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SCK5*
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TP_M_RCV1*
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SMVSWINGH
MCH_SMVSWINGL
MCH_SMVSWINGH
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C6E6 .1UF 10% 16V X7R 603
C6E5 1UF 10% 16V X7R 603
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MCH_HXRCOMP
MCH_HXSWING
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HYSWING
HXRCOMP
HXSWING
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HI_STBF
HI_HLRCOMP
HI_PSWING
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HLSTB*
HLRCOMP
PSWING
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C5R1 1UF 10% 16V X7R 603
C4R7 1UF 10% 16V X7R 603
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HUB I/F
1 OF 5
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DRDY*
DEFER*
HITM*
HIT*
HLOCK*
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BNR*
BPRI*
DBSY*
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RS<1>
RS<0>
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H_TRDY*
H_DRDY*
H_DEFER*
H_HITM*
H_HIT*
H_LOCK*
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H_DBSY*
H_RS<2..0>*
GMCH-CPU, DDR, HUB INTERFACES
DRAWING
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U6E1
MGM7.32

DAC
BLUE C9 VGA_BLUE OUT 8 18
BLUE* D9
GREEN C8 VGA_GREEN OUT 8 18
GREEN* D8
RED A7 VGA_RED OUT 8 18
RED* A8
HSYNC H10 VGA_HSYNC OUT 18
VSYNC J9 VGA_VSYNC OUT 18
REFSET E8 VGA_REFSET IN 10
DDCACLK B6 GLUE4_DDCSCL_3V BI 46
DDCADATA G9 GLUE4_DDCSDA_3V BI 46

LVDS
IYAM<3> C13 3 LVDS_YAM<3..0> OUT 19
IYAM<2> C15 2
IYAM<1> E15 1
IYAM<0> G14 0
IYAP<3> B13 3 LVDS_YAP<3..0> OUT 19
IYAP<2> C14 2
IYAP<1> E14 1
IYAP<0> F14 0
IYBM<3> G11 3 LVDS_YBM<3..0> OUT 19
IYBM<2> C12 2
IYBM<1> E12 1
IYBM<0> H12 0
IYBP<3> G10 3 LVDS_YBP<3..0> OUT 19
IYBP<2> C11 2
IYBP<1> E11 1
IYBP<0> G12 0
ICLKAM D14 LVDS_CLKAM OUT 19
ICLKAP E13 LVDS_CLKAP OUT 19
ICLKBM E10 LVDS_CLKBM OUT 19
ICLKBP F10 LVDS_CLKBP OUT 19
DDCPCLK B4 LVDS_DDCPCLK BI 19
DDCPDATA C5 LVDS_DDCPDATA BI 19
PANELBKLTCTL G8 LVDS_BKLTCTL OUT 19
PANELBKLTEN F8 LVDS_BKLTEN OUT 19
PANELVDDEN A5 LVDS_VDDEN OUT 19
LIBG A10 LVDS_LIBG

CLKS
DREFCLK B7 CK_48M_DOTCLK IN 3
DREFSSCLK B17 CK_66M_LVDS_SS IN 11
LCLKCTLA H9 LCLKCTLA BI 11 19
LCLKCTLB C6 LCLKCTLB BI 11 19

MISC
DPWR* AA22 H_DPWR* OUT 4
DPSLP* Y23 MCH_DPSLP*
RSTIN* AD28 P_PCIRST* IN 24 11 40 45 46 65 66
PWROK J11
EXTTS_0 D6

NC
N/C1 A2
N/C2 A28
N/C3 A29
N/C4 AA9
N/C5 AH1
N/C6 AH29
N/C7 AJ2
N/C8 AJ28
N/C9 AJ29
N/C10 AJ4
N/C11 B1
N/C12 B29

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DVO
17 BI DVOBD<11..0>
DVOBD<11> M5
DVOBD<10> M1
DVOBD<9> N3
DVOBD<8> N2
DVOBD<7> P2
DVOBD<6> N5
DVOBD<5> P5
DVOBD<4> P6
DVOBD<3> R4
DVOBD<2> R6
DVOBD<1> R5
DVOBD<0> R3

17 BI DVOBCLK P3 DVOBCLK
17 BI DVOBCLK* P4 DVOBCLK*
17 BI DVOBHSYNC T6 DVOBHSYNC
17 BI DVOBVSYNC T5 DVOBVSYNC
17 BI DVOBBLANK* L2 DVOBBLANK*
17 BI DVOBFLDSTL M2 DVOBFLDSTL
17 BI DVOBCINTRB G2 DVOBCINTR*
17 BI DVOBCCLKINT M3 DVOBCCLKINT
17 BI DVOCD<11..0>
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DVOCD<10> H6
DVOCD<9> H4
DVOCD<8> H3
DVOCD<7> H1
DVOCD<6> H2
DVOCD<5> J5
DVOCD<4> J6
DVOCD<3> K2
DVOCD<2> K3
DVOCD<1> K1
DVOCD<0> K5

17 BI DVOCCLK J3 DVOCCLK
17 BI DVOCCLK* J2 DVOCCLK*
17 BI DVOCHSYNC K6 DVOCHSYNC
17 BI DVOCVSYNC L5 DVOCVSYNC
17 BI DVOCBLANK* L3 DVOCBLANK*
17 BI DVOCFLDSTL H5 DVOCFLDSTL

17 BI MI2CCLK K7 MI2CCLK
17 BI MI2CDATA N6 MI2CDATA
17 BI MDVICLK N7 MDVICLK
17 BI MDVIDATA M6 MDVIDATA
17 BI MDDCCLK P7 MDDCCLK
17 BI MDDCDATA T7 MDDCDATA
17 BI ADDID<7..0>
ADDID<7> F6
ADDID<6> G6
ADDID<5> F4
ADDID<4> G5
ADDID<3> E2
ADDID<2> E3
ADDID<1> F5
ADDID<0> E5

17 11 BI DVODETECT L7 DVODETECT
17 BI DPMS_CLK D5 DPMS
F1 GVREF
AGP_BUSY* F7 AGPBUSY*
10 BI MCH_DVORCOMP D1 DVORCOMP
3 BI CK_66M_GMCH Y3 GCLKIN

RSVD1 AA5 RSVD1
RSVD2 B12 RSVD2
17 BI ADD_RSVD_A8 B2 RSVD3
17 BI ADD_RSVD_B8 B3 RSVD4
17 11 BI AGP_ST2 C2 RSVD5
RSVD6 D12 RSVD6
17 BI ADD_RSVD_A14 D2 RSVD7
17 BI ADD_RSVD_B12 D3 RSVD8
RSVD9 D7 RSVD9
RSVD10 F12 RSVD10
17 BI ADD_RSVD_B18 F2 RSVD11
17 BI ADD_RSVD_A18 F3 RSVD12
17 BI ADD_RSVD_B39 L4 RSVD13

17 11 BI AGP_ST1 C3 GST<1>
17 11 BI AGP_ST0 C4 GST<0>

17 11 9 8 58 68 67 56 24 23 IN V_1P5_CORE
R4P6 100K 1% CH 603
R3E4 100K 1% CH 603
R4E3 100K 1% CH 603
R4D5 100K 1% CH 603
C4P3 .1UF 10% 16V X7R 603
VCC3
R4P5 8.2K 5% CH 603
AGP_BUSY*

R6D2 1.5K 1% CH 603
VCCP
R3R2 1K 5% CH 603
R4P9 0 603 1A CH
CPU_VR_PWRGD IN 59 3
MCH_EXTTS IN 11

18 8 IN VGA_BLUE
18 8 IN VGA_GREEN
18 8 IN VGA_RED
MMBD7000LT1
Q5C1 GP SOT23S DIO
Q5D2 GP SOT23S DIO
Q5D1 GP SOT23S DIO
23 17 11 9 8 58 68 67 56 24 IN V_1P5_CORE
C5D1 .1UF 5% 16V X7R 603
C5D3 .1UF 5% 16V X7R 603
C5D2 .1UF 5% 16V X7R 603
VGA CLAMPING DIODES

GMCH-VIDEO, CLKS, CTRL, POWER, GND

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GMCH-POWER AND GROUNDS

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GND
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IC

U6E1
MGM732
POWER
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IC

V_1P3_GMCH
V_1P5_GMCH_DPLLA
V_1P5_GMCH_DPLLB
V_1P5_CORE
V_2P5_CORE
V_2P5_SM
VCCP
VCC3

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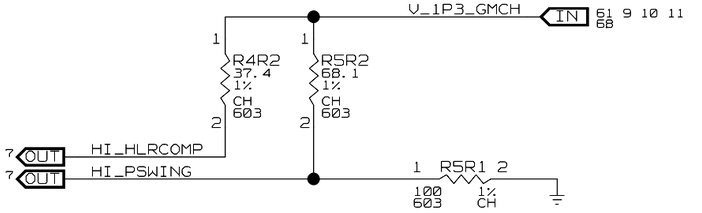
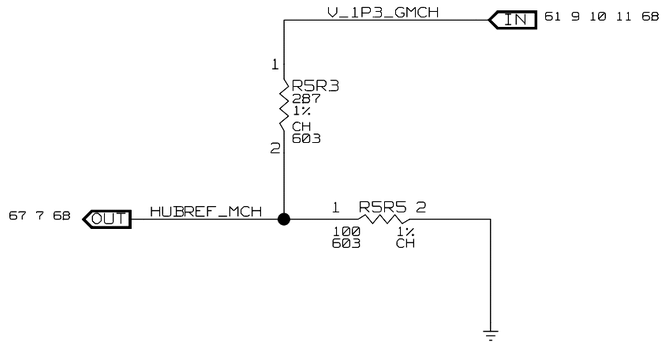
855GMEFB.SCH_1.9
Wed Apr 13 15:32:46 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	9	C3

HUBLINK



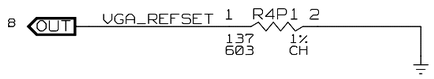


GMCH CORE VOLTAGE TABLE

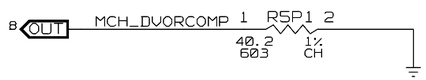
RESISTOR	1.2V	1.35V
R6R3	243, 1%	287, 1%
R5R3	27.4, 1%	37.4, 1%
R6R2	49.9, 1%	68.1, 1%

NOTE: SEE PG61 FOR RELATED STUFFING OPTIONS

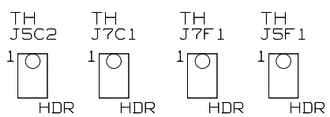
DAC



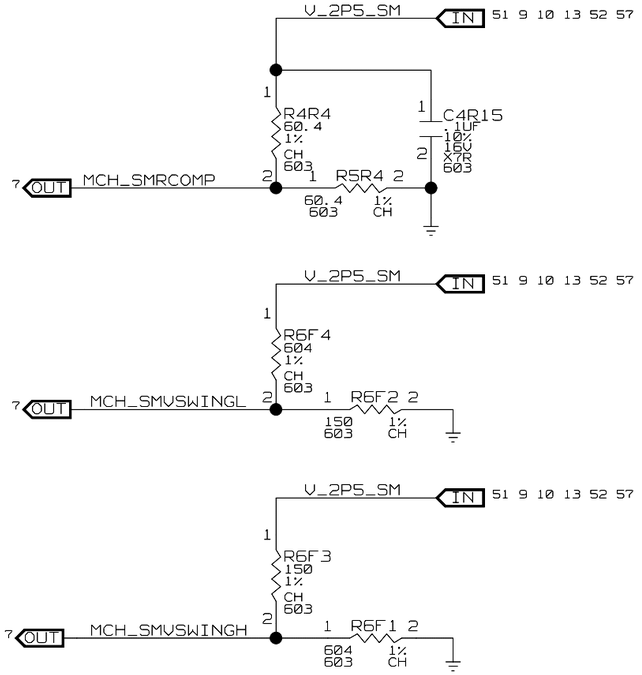
DVO



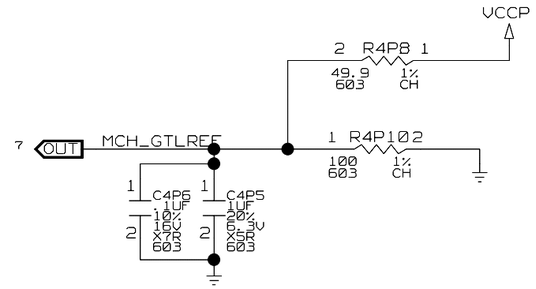
HEATSINK RETENTION CLIPS: QTY(4)



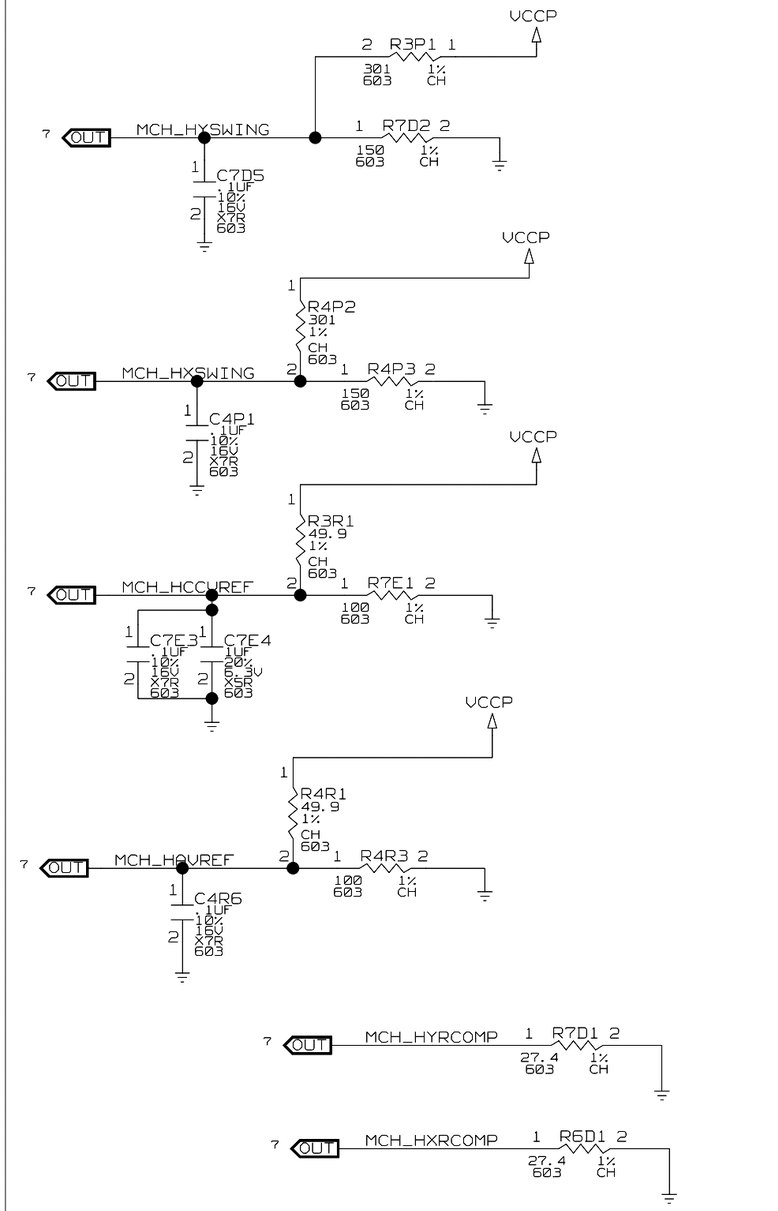
MEMORY



GTL



MCH COMPENSATION & REFERENCE VOLTAGE

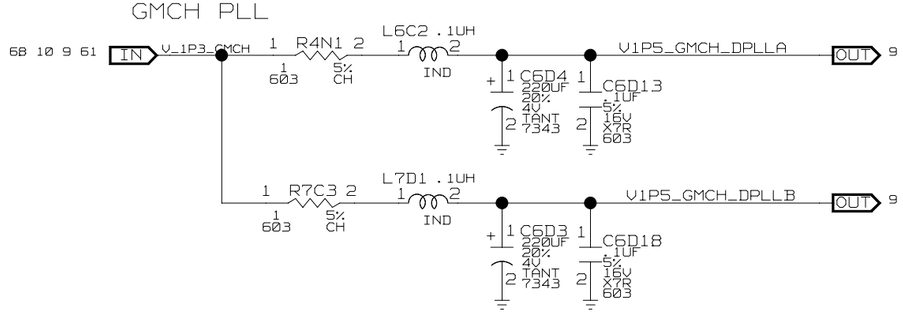


GMCH-CIRCUITRY

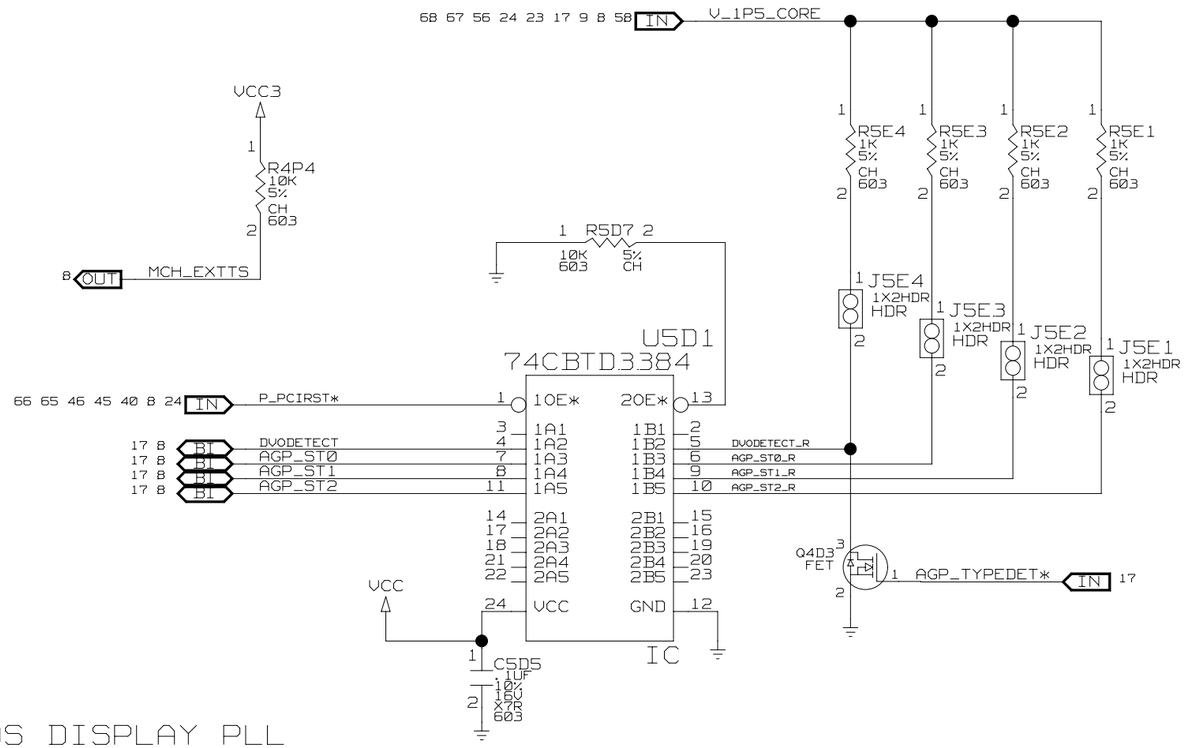
DRAWING
855GMEFB.SCH_1.10
Wed Apr 13 15:32:47 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	10	C3

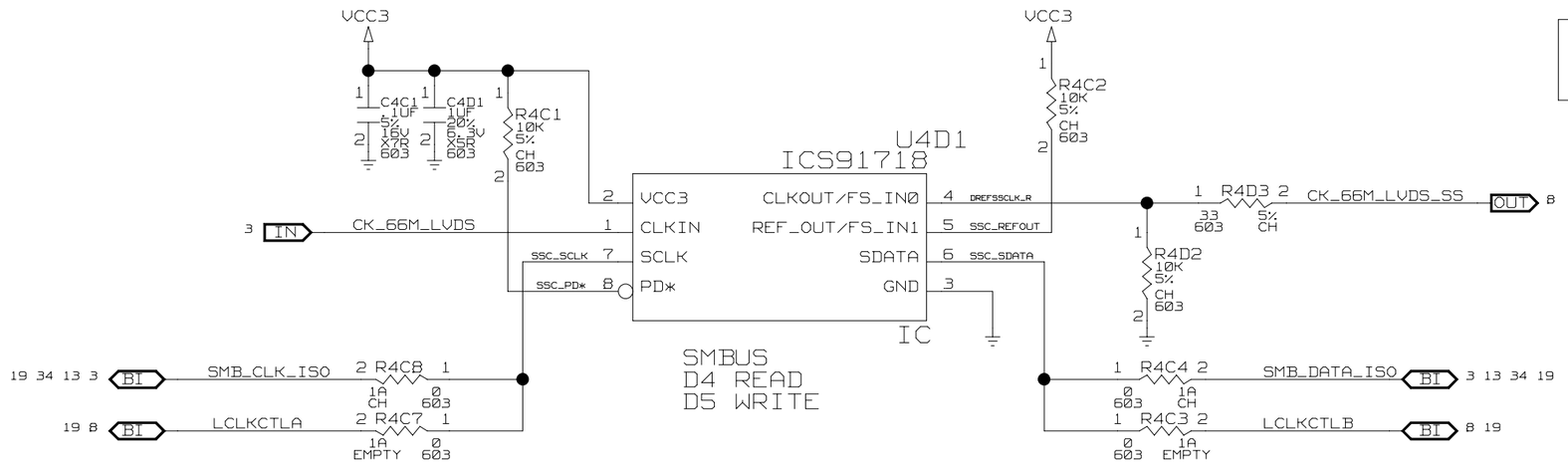
GMCH PLL



GMCH STRAPPING OPTIONS



SPREAD SPECTRUM CLOCK GENERATOR FOR LVDS DISPLAY PLL



GMCH STRAPPING OPTIONS

	FUNCTION	BOARD DEFAULT	OPTION OVERRIDE
J5E4	DVO/AGP STRAP	NO SHUNT FOR DVO	SHUNT FOR AGP 4X

J5E1	J5E2	J5E3	PSB FREQ	SM FREQ	GFX FREQ
0	0	0	400	266	200
0	0	1	400	200	200
0	1	0	400	200	133
1*	1*	1*	400	333	250

0 = NO SHUNT, 1 = SHUNT
* = DEFAULT

GMCH PLL, STRAPS & MISC CLKS

DRAWING
855GMEFB.SCH_1.11
Wed Apr 13 15:32:47 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	11	C3

ROOM=DCL_DDR_CORE

M_CB_RS<7..0> BI 13 15

M_DQS_RS<8..0> OUT 13 14

M_DM_RS<8..0> BI 13 14

M_DQ_RS<63..0> BI 13 14

7 BI M_CB<7..0>

7 IN M_DQS<8..0>

7 BI M_DM<8..0>

7 BI M_DQ<63..0>

RP6F4 10 SM 5% IC

RP6F4 10 SM 5% IC

RP6F3 10 SM 5% IC

RP6F3 10 SM 5% IC

RP6F4 10 SM 5% IC

RP6F4 10 SM 5% IC

RP6F3 10 SM 5% IC

RP6F3 10 SM 5% IC

R6F6 10 603 5% CH

R8F8 10 5% CH

R7F6 10 5% CH

R7F4 10 5% CH

R7F1 10 5% CH

R6F8 10 5% CH

R5F5 10 5% CH

R5F3 10 5% CH

R5F2 10 5% CH

R6F7 10 603 5% CH

R8F7 10 5% CH

R7F5 10 5% CH

R7F3 10 5% CH

R7F2 10 5% CH

R6F9 10 5% CH

R5F6 10 5% CH

R5F4 10 5% CH

R5F1 10 5% CH

RP8F2 10 5% IC

RP8F2 10 5% IC

RP8F1 10 5% IC

RP8F1 10 5% IC

RP8F2 10 5% IC

RP8F2 10 5% IC

RP8F1 10 5% IC

RP8F1 10 5% IC

RP7F6 10 5% IC

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RP5F1 10 5% IC

RP5F1 10 5% IC

RP4F1 10 5% IC

RP4F1 10 5% IC

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RP4F1 10 5% IC

DDR SERIES RESISTORS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.12 Wed Apr 13 15:32:48 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	12	C3

ROOM=DCL_DDR_CORE

DDR DIMM 0

PRIMARY A13373-002
ALTERNATE A13373-001

J4G1
DIMM2P_184_CK

DDR DIMM 1

PRIMARY A13373-002
ALTERNATE A13373-001

J4G2
DIMM2P_184_CK

CONN

M_DQ_RS<63..0>
M_WE*
M_RAS*
M_CAS*
M_MAA<12..0>
M_MAA_CPC<5..1>
M_DM_RS<8..0>
M_DQS_RS<8..0>
M_CB_RS<7..0>
M_SCS<3..0>*
M_SCKE<3..0>
M_BS<1..0>
SMB_DATA_ISO
SMB_CLK_ISO
V_2P5_SM
V_2P5_CORE
DIMM_VREF_1P25

CK_M_100_133M_P_DDR0
CK_M_100_133M_N_DDR0
CK_M_100_133M_P_DDR1
CK_M_100_133M_N_DDR1
CK_M_100_133M_P_DDR2
CK_M_100_133M_N_DDR2
CK_M_100_133M_P_DDR3
CK_M_100_133M_N_DDR3
CK_M_100_133M_P_DDR4
CK_M_100_133M_N_DDR4
CK_M_100_133M_P_DDR5
CK_M_100_133M_N_DDR5

R6U1 49.9 1% CH 603
R6U2 49.9 1% CH 603
PLACE RES DIVIDER NEAR DIMMS

C4G1 .1UF 10% 16V X7R 603
C6U2 .1UF 10% 16V X7R 603
NEAR DIMM PIN

DDR DIMMS

DRAWING 855GMEFB.SCH_1.13
Wed Apr 13 15:32:49 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	13	C3

ROOM=DCL_DDR_CORE

16 15 52 IN V_1P25_MEMVTT

13 12 IN M_DQS_RS<8..0>

13 12 BI M_DM_RS<8..0>

13 12 BI M_DQ_RS<63..0>

13 7 BI M_MAA<12..0>

R4U6 2 — 56 603 5% CH

RP8G2 — 56 SM — 5% .063W IC

RP7G8 — 56 SM — 5% .063W IC

R3U1 2 — 56 603 5% CH

R3U5 2 — 56 603 5% CH

RP6G3 — 56 SM — 5% .063W IC

RP5G7 — 56 SM — 5% .063W IC

RP5G3 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP8G3 — 56 SM — 5% .063W IC

RP8G2 — 56 SM — 5% .063W IC

RP8G1 — 56 SM — 5% .063W IC

RP8G3 — 56 SM — 5% .063W IC

RP8G2 — 56 SM — 5% .063W IC

RP8G1 — 56 SM — 5% .063W IC

RP7G8 — 56 SM — 5% .063W IC

RP7G8 — 56 SM — 5% .063W IC

RP7G7 — 56 SM — 5% .063W IC

RP7G7 — 56 SM — 5% .063W IC

RP8G1 — 56 SM — 5% .063W IC

RP7G7 — 56 SM — 5% .063W IC

RP7G7 — 56 SM — 5% .063W IC

RP7G6 — 56 SM — 5% .063W IC

RP7G6 — 56 SM — 5% .063W IC

RP7G3 — 56 SM — 5% .063W IC

RP7G3 — 56 SM — 5% .063W IC

RP7G6 — 56 SM — 5% .063W IC

RP7G6 — 56 SM — 5% .063W IC

R3U2 2 — 56 603 5% CH

RP7G3 — 56 SM — 5% .063W IC

RP7G2 — 56 SM — 5% .063W IC

RP7G2 — 56 SM — 5% .063W IC

RP7G1 — 56 SM — 5% .063W IC

RP7G1 — 56 SM — 5% .063W IC

RP7G3 — 56 SM — 5% .063W IC

RP7G2 — 56 SM — 5% .063W IC

RP7G1 — 56 SM — 5% .063W IC

RP7G1 — 56 SM — 5% .063W IC

RP6G4 — 56 SM — 5% .063W IC

RP6G4 — 56 SM — 5% .063W IC

RP6G3 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP6G4 — 56 SM — 5% .063W IC

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RP6G1 — 56 SM — 5% .063W IC

RP5G6 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP5G6 — 56 SM — 5% .063W IC

RP5G6 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G3 — 56 SM — 5% .063W IC

RP5G3 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G2 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP4G1 — 56 SM — 5% .063W IC

RP4G1 — 56 SM — 5% .063W IC

RP5G2 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP4G1 — 56 SM — 5% .063W IC

RP4G1 — 56 SM — 5% .063W IC

R5U2 2 — 56 603 5% CH

RP5G7 — 56 SM — 5% .063W IC

RP6G6 — 56 SM — 5% .063W IC

RP5G7 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

R4U3 2 — 56 603 5% CH

R4U1 2 — 56 603 5% CH

RP6G6 — 56 SM — 5% .063W IC

DDR TERMINATION RESISTORS

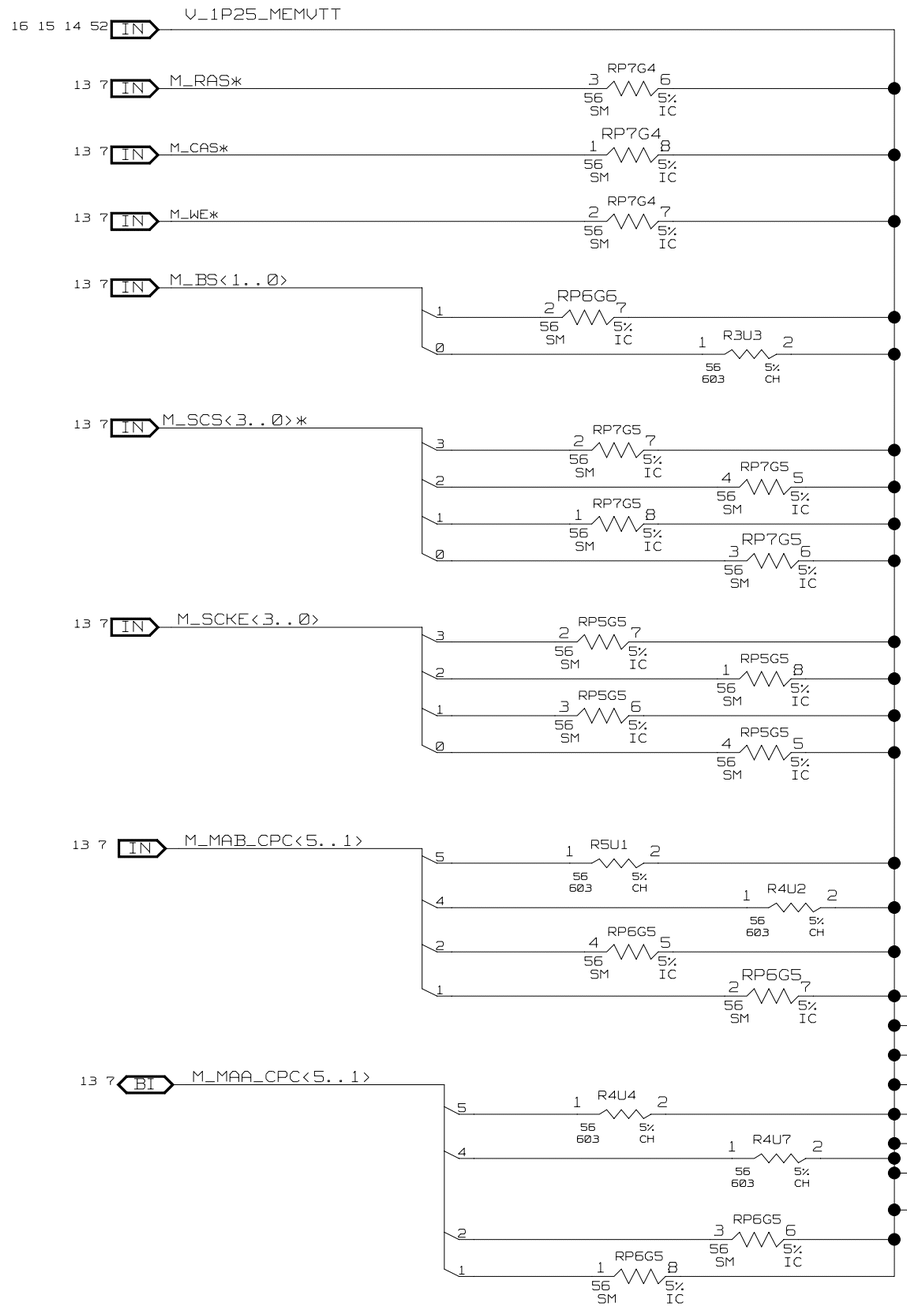
DRAWING
855GMEFB.SCH_1.14
Wed Apr 13 15:32:49 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	14	C3

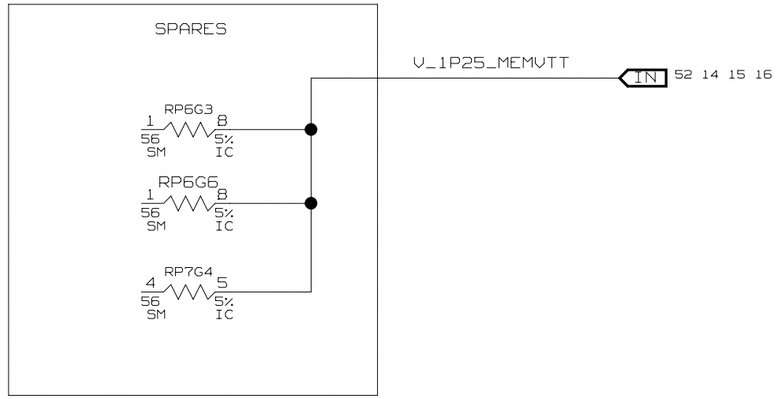
NOTE:

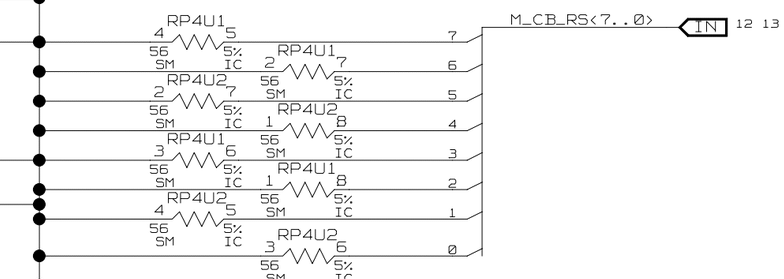
CS SIGNALS MUST HAVE IT'S OWN RES/RPACK
CKE SIGNALS MUST HAVE IT'S OWN RES/RPACK
CPC SIGNALS MUST HAVE IT'S OWN RES/RPACK

ROOM=DCL_DDR_CORE



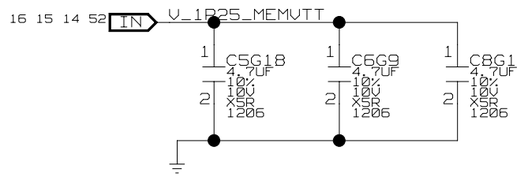
SPARES



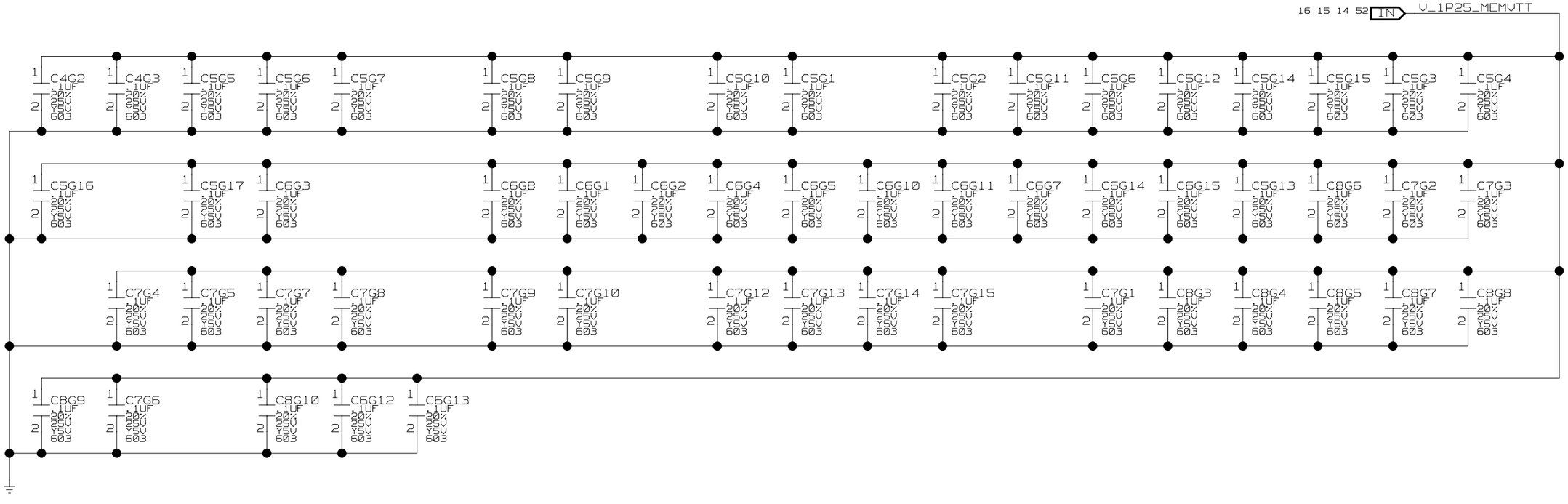


DDR TERMINATION RESISTORS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.15 Wed Apr 13 15:32:50 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	15	C3



PLACED AT LEFT, CENTER AND RIGHT
OF VTT ISLAND



DDR DECOUPLING CAPACITORS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.16 Wed Apr 13 15:32:50 2005	5200 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	16	C3

ROOM=DCL_CORE_AGP

J4C2
1.5V CONAGP

AGP_ST2 B11 ST2
AGP_ST1 A10 ST1
AGP_ST0 B10 ST0
DVOCFLDSTL B26 GAD31
DVOBCINTRB A26 GAD30
B27 GAD29
A27 GAD28
B29 GAD27
A29 GAD26
B30 GAD25
A30 GAD24
B33 GAD23
A35 GAD22
B35 GAD21
A36 GAD20
DVOCD<11..0> B36 GAD19
DVOCBLANK* A38 GAD18
DVOCHSYNC B38 GAD17
DVOCVSYNC A39 GAD16
MDDCDATA A51 GAD15
DVOBFLDSTL B53 GAD14
DVOBCCLKINT A53 GAD13
B54 GAD12
A54 GAD11
B56 GAD10
A56 GAD9
B57 GAD8
B60 GAD7
A60 GAD6
B62 GAD5
A62 GAD4
DVOBD<11..0> B63 GAD3
A63 GAD2
DVOBVSYNC B65 GAD1
DVOBHSYNC A65 GAD0
DVOBCLK B59 GAD_STB0
DVOCCLK B32 GAD_STB1
DVOBCLK* A59 GAD_STB0
DVOCCLK* A32 GAD_STB1
ADD_RSVD_B18 B18 SB_STB
ADD_RSVD_A18 A18 SB_STB
DVOCD<5> A33 GC_BE3
ADD_RSVD_B39 B39 GC_BE2
DVOBBLANK* B51 GC_BE1
DVOBD<7> A57 GC_BE0
B4 USB+
A4 USB-
P_INTA* A6 INTA
P_INTB* B6 INTB
CK_66M_AGP B7 AGPCLK
P_RST_SLOTS* A7 PCIRST
B1 OVRCNT
AGP_TYPEDET* A2 TYPEDET
P_PME* A48 PME

GDEVSEL B46 MI2CDATA
GTRDY A46 MDVICLK
GIRDY B41 MI2CCLK
GFRAME A41 MDVIDATA
GSTOP A47 MDDCCLK
GPERR B48 ADD_PERR*
GSERR B50 ADD_SERR*
GPAR A50 DVODETECT
WBF A14 ADD_RSVD_A14
GREQ B8 ADD_RSVD_B8
GGNT A8 ADD_RSVD_A8
RBF B12 ADD_RSVD_B12
PIPE A12 DPMS_CLK
12V A1
VCC B2
VCC B3
VCC3 A9
VCC3 B9
VCC3 A16
VCC3 B16
VCC3 A28
VCC3 B28
VCC3 A25
VCC3 B25
VDDQ A34
VDDQ B34
VDDQ A40
VDDQ B40
VDDQ B47
VDDQ A52
VDDQ B52
VDDQ A58
VDDQ B58
VDDQ A64
VDDQ B64
SBA7 A21
SBA6 B21
SBA5 A20
SBA4 B20
SBA3 A17
SBA2 B17
SBA1 A15
SBA0 B15
3.3VAUX B24 V_3P3_PCIVAUX
VREFGC A66
VREFCG B66
RSVD A3
RSVD A11
RSVD B14
RSVD A22
RSVD B22
RSVD A24

CONN

NC=1, 2, 3
GND=A5, B5, A13, B13, A19, B19, A23, B23, A31, B31, A37, B37, A49, B49, A55, B55, A61, B61

V_1P5_CORE IN 58 8 9 11 17 23 24 56 67 68
R3E1 8.2K 1% CH 603
R3E2 8.2K 1% CH 603
+12V
VCC
VCC3
ADDID<7..0> IN 8
R4E7 1K 1% CH 603
DVO_VREF OUT 8
R4P7 1K 1% CH 603
C4E5 .1UF 10% X7R 603 PLACE NEAR ADD SLOT

68 67 56 24 23 17 11 9 8 58 IN V_1P5_CORE
MDDCDATA R4E2 2.2K 603 5% CH
MI2CDATA R6R1 2.2K 603 5% CH
MDVIDATA R6P1 2.2K 603 5% CH
MI2CCLK R4D6 2.2K 603 5% CH
MDVICLK R6R2 2.2K 603 5% CH
MDDCCLK R4E1 2.2K 603 5% CH

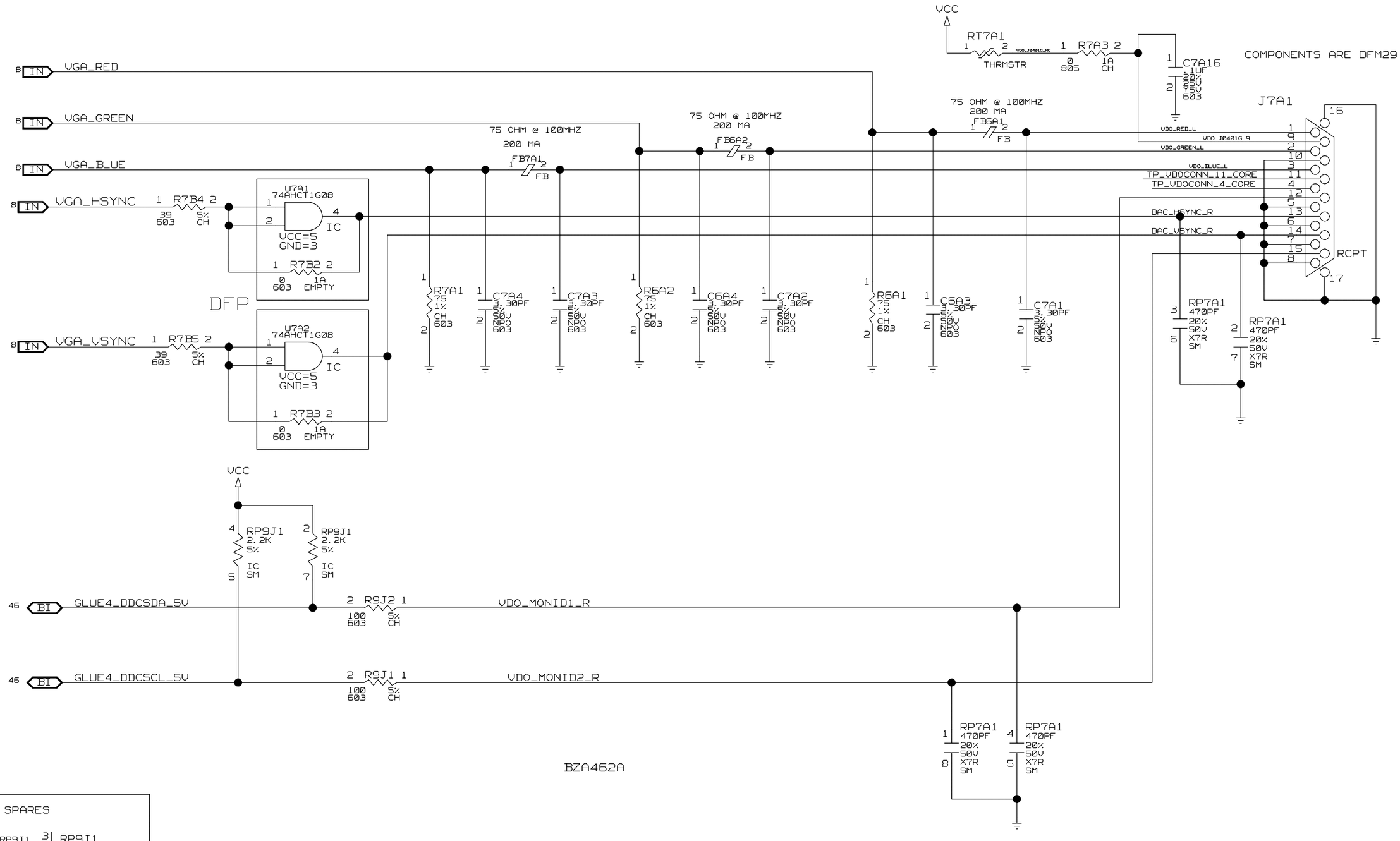
AGP CONNECTOR DECOUPLING
V_1P5_CORE IN 58 58 8 9 11 17 23 24 56 67
C4E3 150UF 20% 10V EMPTY 7343
C4E2 150UF 20% 10V EMPTY 7343
C4E1 100UF 20% 10V TANT 7343
C4D4 22UF 20% 10V TANT 3528
C6P3 .1UF 5% 16V X7R 603
C6P2 .1UF 5% 16V X7R 603
C3D7 .1UF 5% 16V X7R 603
C3D10 .1UF 5% 16V X7R 603
C3E6 .1UF 5% 16V X7R 603
C6R2 .1UF 5% 16V X7R 603
C6R1 .1UF 5% 16V X7R 603
VCC
C3C6 22UF 20% 10V TANT 3528
C3C5 1UF 5% 16V X7R 603
C7N1 5% 16V X7R 603
VCC3
C4C2 100UF 20% 10V TANT 7343
C4D3 22UF 20% 10V TANT 3528
C3C9 22UF 20% 10V TANT 3528
C3D5 1UF 5% 16V X7R 603
C3D1 1UF 5% 16V X7R 603
C6P1 1UF 5% 16V X7R 603
CAD NOTE: PLACE NEAR AGP CONNECTOR

68 67 56 24 23 17 11 9 8 58 IN V_1P5_CORE
R8W1 1K 603 5% CH
DPMS_CLK_R
Q4D1 FET
Q4D2 FET
DPMS_CLK OUT 8 17
Q2J1 FET
40 21 IN SUSCLK
+12V
R4D4 100K 603 5% CH
11 17 IN AGP_TYPEDET*

AGP DIGITAL DISPLAY

DRAWING
855GMEFB.SCH_1.17
Wed Apr 13 15:32:51 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	17	C3



DRAWING
855GMEFB.SCH_1.18
Wed Apr 13 15:32:51 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	18	C3

VGA CONNECTOR

LVDS PANEL BACKLIGHT

LVDS CONNECTOR

BIOS NOTE:
DISABLE BOTH BKLTSEL
LINES BEFORE ENABLING ONE

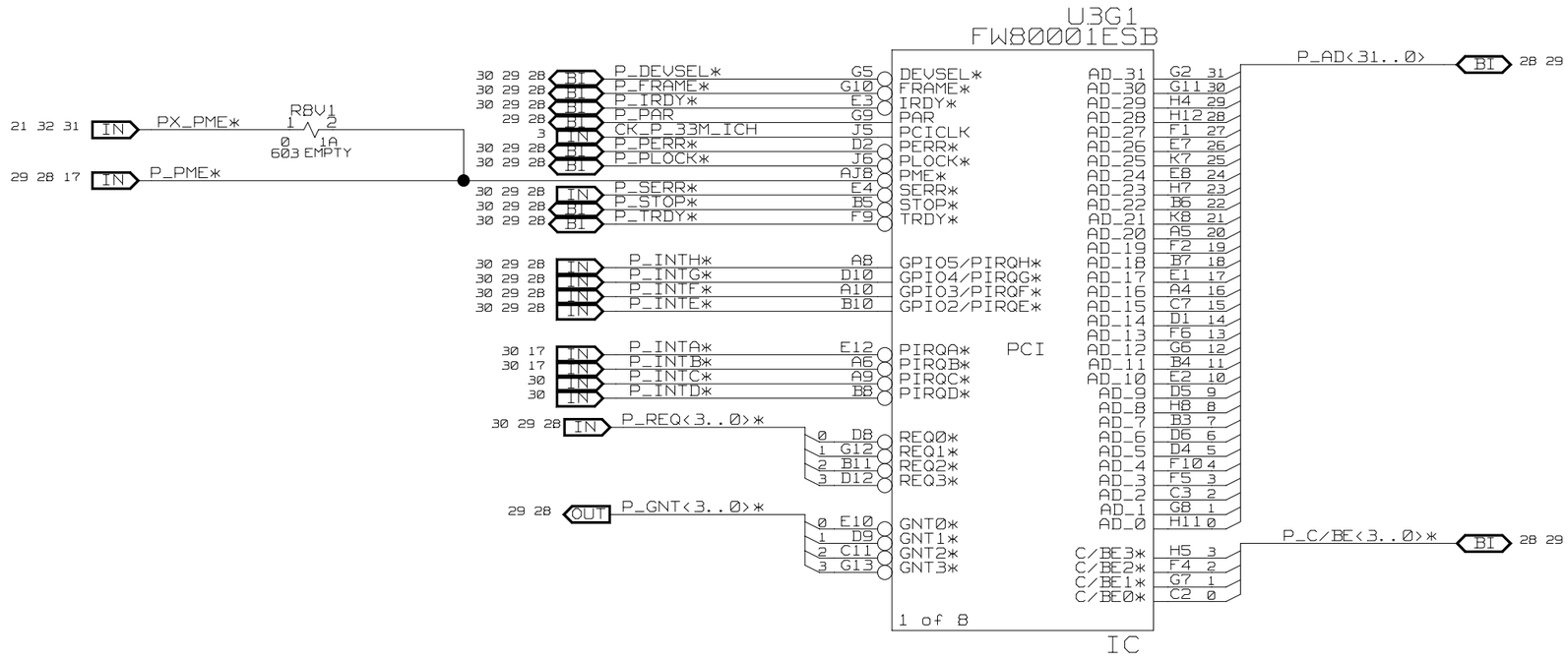
STUFFING OPTIONS
FOR 3.3V/12V
BACKLIGHT SUPPORT

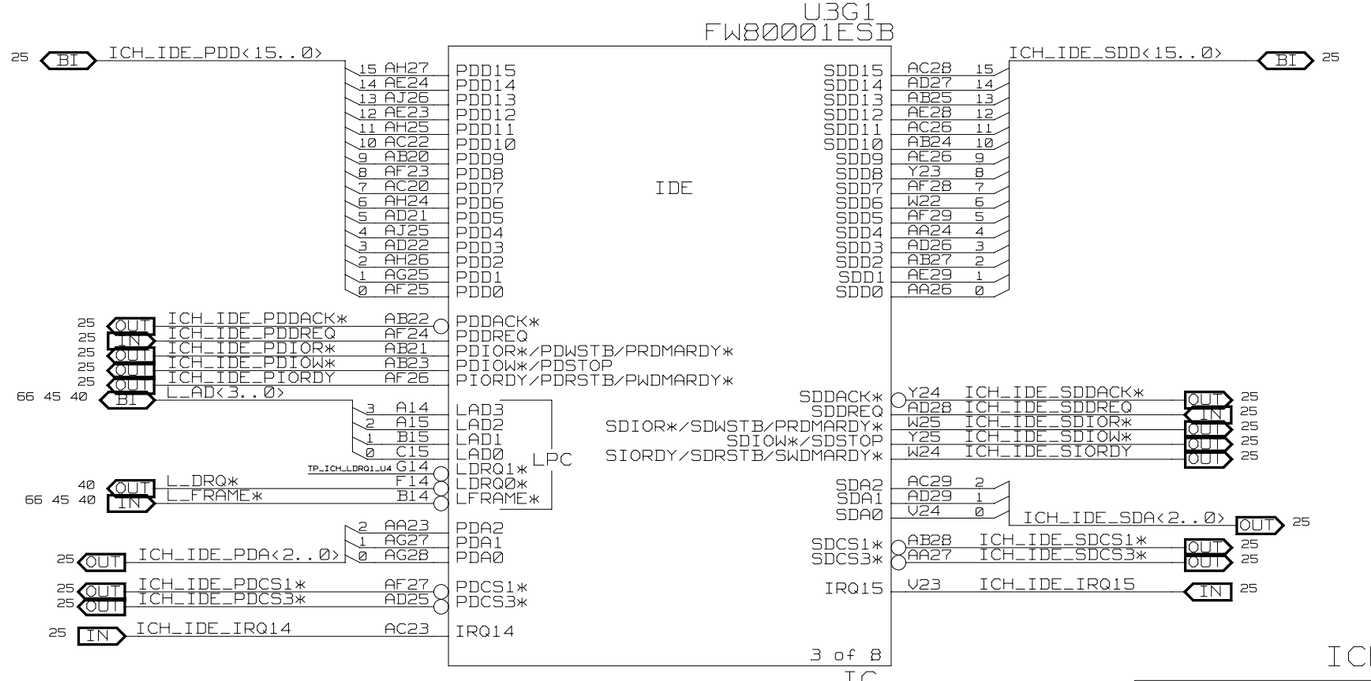
J5A2
CONN30P_LVDS

J5C1
7PIN HDR

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 19	REV C3

DRAWING
855GMEFB.SCH_1.19
Wed Apr 13 15:32:51 2005

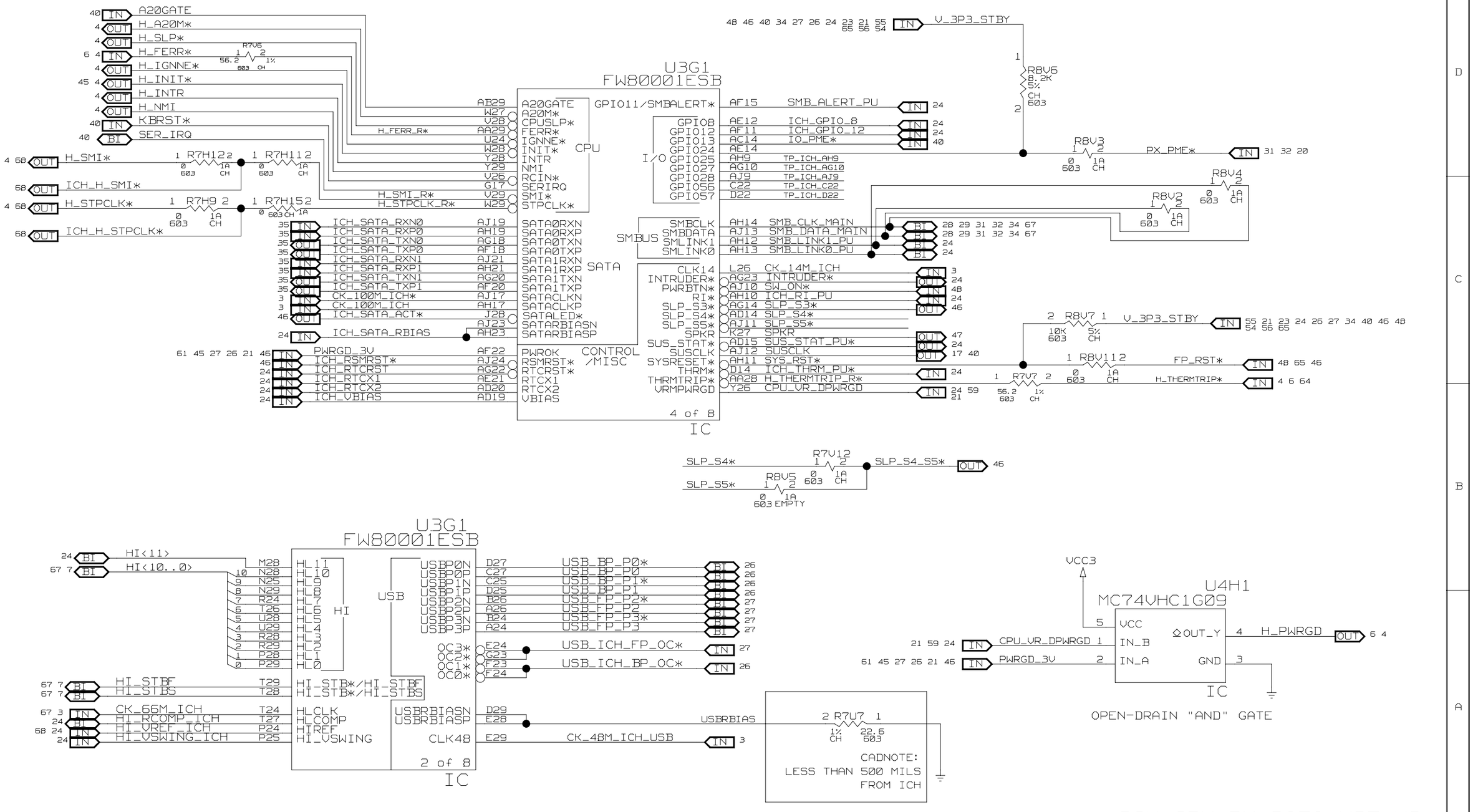




ICH PCI, IDE

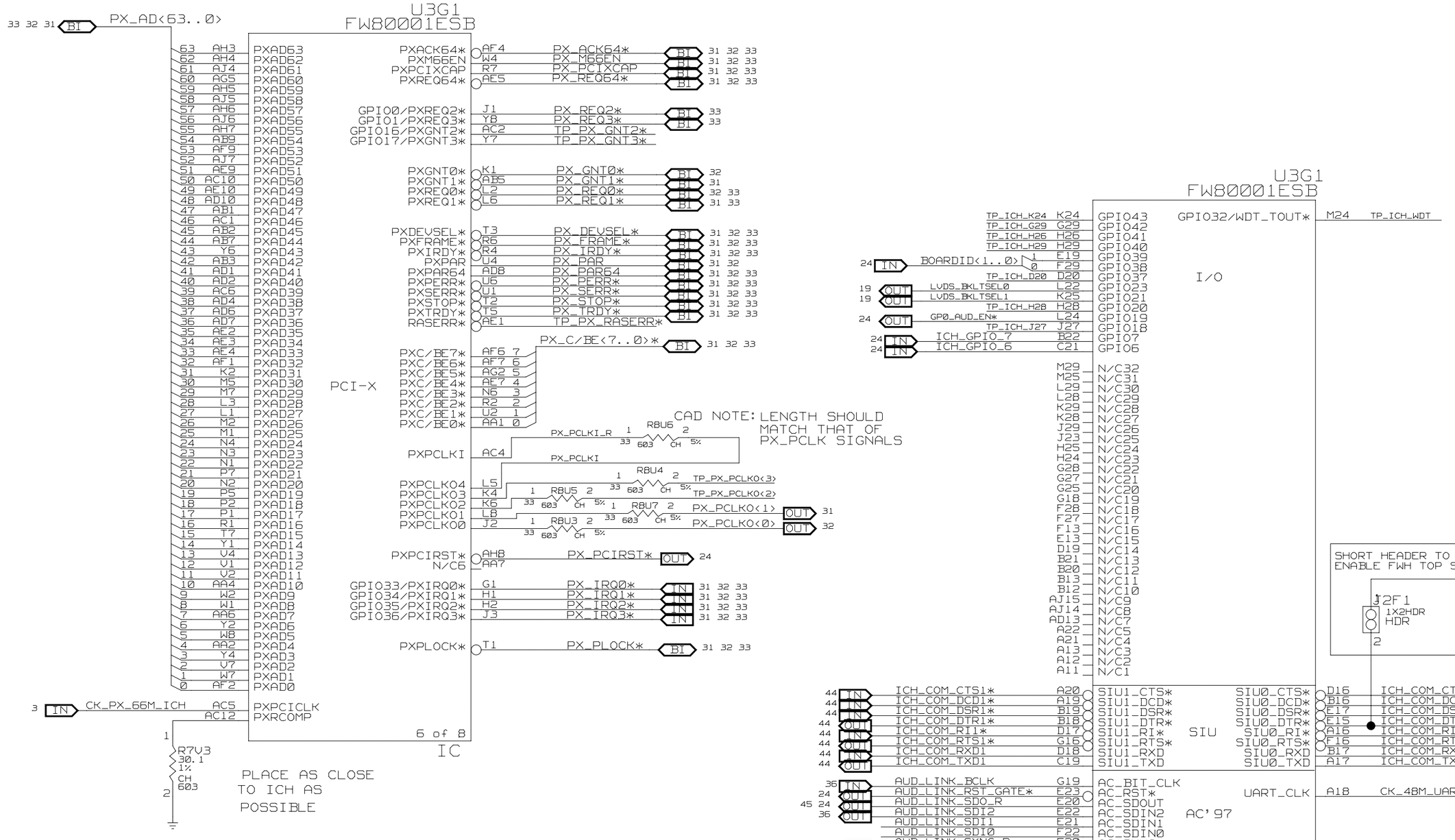
DRAWING
855GMEFB.SCH_1.20
Wed Apr 13 15:32:52 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	20	C3

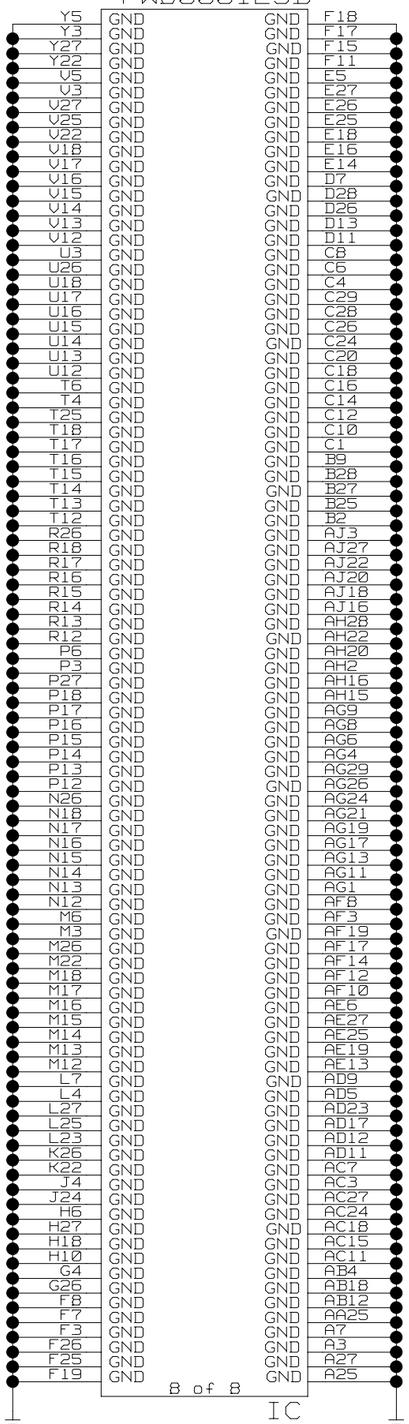


ICH CPU, PM, SATA, USB, HI

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.21 Wed Apr 13 15:32:52 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	21	C3



DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.22 Wed Apr 13 15:32:53 2005	5200 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	22	C3



ICH POWER, GND

DRAWING				
855GMEFB.SCH.1.23 Wed Apr 13 15:32:53 2005	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 23	REV C3

VCC3

R7U8 10K 5% EMPTY 603
R7T4 10K 5% EMPTY 603
R7U9 2.7K 5% CH 603
R7U6 2.7K 5% CH 603

BOARDID<1..0> OUT 22

22 IN PX_PCIRST*

DEBUG ONLY
R8V9 0 603 1A CH

P_PCIRST* OUT 8 11 40 45 46 65 66

C8V10 47PF 5% 50V NP0 603

48 46 40 34 27 26 24 23 21 55 65 56 54 IN V_3P3_STBY

Q1G1
BAT54C SOT23C DIO

BH1G1 3PCOIN

VREG_VBAT_R R1G2 1K 603 5% CH

V_3P0_BAT_VREG OUT 23 24

C1G2 1UF 5% 16V X7R 603
C1G1 1UF 5% 16V X7R 603

CAD NOTE: PLACE NEAR ICH

V_BAT_VREG_R_CR OUT 24

THROUGH-HOLE

CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS

ATTRIBUTES:

23 24 IN V_3P0_BAT_VREG C7V17 .1UF 20% 25V Y5V 603

23 46 IN V_REF5V C8U1 .1UF 20% 25V Y5V 603

23 46 IN V_REF5V_SUS C7U3 .1UF 20% 25V Y5V 603

TERMINATION FOR INTEGRATED AUDIO

45 22 IN AUD_LINK_SDO_R R7U1 33 603 5% CH AUD_LINK_SDO_CODEC OUT 36

22 IN AUD_LINK_SYNC_R R7U5 33 603 5% CH AUD_LINK_SYNC_CODEC OUT 36

VCC3

R7U3 8.2K 5% CH 603
R7U4 8.2K 5% CH 603
R7U8 8.2K 5% CH 603
R7U2 8.2K 5% CH 603

ICH_THRM_PU* OUT 21
CPU_VR_DPWRGD OUT 59 21
ICH_GPIO_6 OUT 22
ICH_GPIO_7 OUT 22
HI<11> OUT 21
ICH_SATA_RBIAS OUT 21

R7U17 56.2 1% CH 603
R7U9 24.9 1% CH 603

SPARE GATES

U2B1 74LVC00A IC VCC3=14 GND=7
U2B1 74LVC00A IC VCC3=14 GND=7

AC97 RESET CIRCUIT

22 IN AUD_LINK_RST_GATE*
22 IN GP0_AUD_EN*
U2B1 74LVC00A IC VCC3=14 GND=7
U2B1 74LVC00A IC VCC3=14 GND=7
AUD_LINK_RST* OUT 36

23 24 IN V_3P0_BAT_VREG

R4H4 1M 603 5% CH
J4J1 1X2HDR HDR
INTRUDER HDR
INTRUDER* OUT 21
ICH_RTCRST OUT 21

R4J1 180K 603 5% CH
C3J1 1UF 5% 16V X7R 603

J3J1 1X3HDR HDR
TP_CLRCMOS
NET_CLR_CMOS_JUMPER
R3H1 4.7K 5% CH 603

1-2	NORMAL
2-3	CLR CMOS

V_3P3_STBY IN 55 21 23 24 26 27 34 40 46 48

R7U18 8.2K 5% CH 603
R8U14 8.2K 5% CH 603
R7U13 10K 5% CH 603
R7U14 10K 5% CH 603
R8U8 8.2K 5% CH 603
R7U11 10K 5% CH 603
R7U10 10K 5% EMPTY 603

SUS_STAT_PU* OUT 21
SMB_ALERT_PU OUT 21
ICH_RI_PU OUT 21
SMB_LINK1_PU OUT 21
SMB_LINK0_PU OUT 21
ICH_GPIO_12 OUT 21
ICH_GPIO_8 OUT 21

68 67 56 23 17 11 9 8 58 IN V_1P5_CORE

R6V2 75 1% CH 603
R7V1 43.2 1% CH 603
R7V2 48.7 1% CH 603
R6V1 22.6 1% CH 603
R7U18 49.9 1% CH 603

HI_RCOMP_ICH OUT 21
HI_VSWING_ICH OUT 21
HI_VREF_ICH OUT 68 21

C7U14 C7U12 C6U5 C6U4 .1UF 5% 16V X7R 603

24 IN V_BAT_VREG_R_CR
C7W1 .047UF 20% 50V X7R 603
C7W2 1UF 10% 16V EMPTY 603

ICH_VBIAS OUT 21
R7W1 10M 603 5% CH
ICH_RTCX1 OUT 21
ICH_RTCX2 OUT 21

AS2705-003
XY3J1 SOCKET
TH CONN

NOTE:
ADD XTAL PART # 107930-002 TO BOM WITH MOD FILE

R7V171 10M 603 5% CH
C3H2 10PF 5% 50V NP0 603
C3H1 10PF 5% 50V NP0 603

ICH STRAPPING & DECOUPLING

DRAWING
855GMEFB.SCH_1.24
Wed Apr 13 15:32:54 2005

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	30117601	24	C3

DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS

VCC3

R5V4 2 1 4.7K 603 5%

R5V3 2 1 8.2K 603 5%

R5V2 2 1 4.7K 603 5%

R5V1 2 1 8.2K 603 5%

46 IN IDE_RST*

20 OUT ICH_IDE_PDDREQ
20 IN ICH_IDE_PDIOW*
20 IN ICH_IDE_PDIOR*
20 OUT ICH_IDE_PIORDY
20 IN ICH_IDE_PDDACK*
20 OUT ICH_IDE_IRQ14
20 IN ICH_IDE_PDA<1>
20 IN ICH_IDE_PDA<0>
20 IN ICH_IDE_PDCS1*
20 IN ICH_IDE_PDCS3*
20 IN ICH_IDE_PDA<2>

20 IN ICH_IDE_SDD<15..0>
20 IN ICH_IDE_PDD<15..0>

R4H3 2 1 33 603 5% CH

R4H2 2 1 33 603 5% CH

J4H2
2X20HDR_20
IDE_PRI_RST_R

J4H1
2X20HDR_20
IDE_SEC_RST_R

HDR
TP_IDE_PRI_32
TP_IDE_SEC_32

PRIMARY IDE CONNECTOR

GPIO_DMA66_DETECT_PRI OUT 45
IDE_PRI_ACT* OUT 46

R4V2 2 1 15K 603 5%

C5V2 1 2 .047UF 20% 50V EMPTY 603 "X7R" (+/- 10%)

CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN

SECONDARY IDE CONNECTOR

GPIO_DMA66_DETECT_SEC OUT 45
IDE_SEC_ACT* OUT 46

R4V1 2 1 15K 603 5%

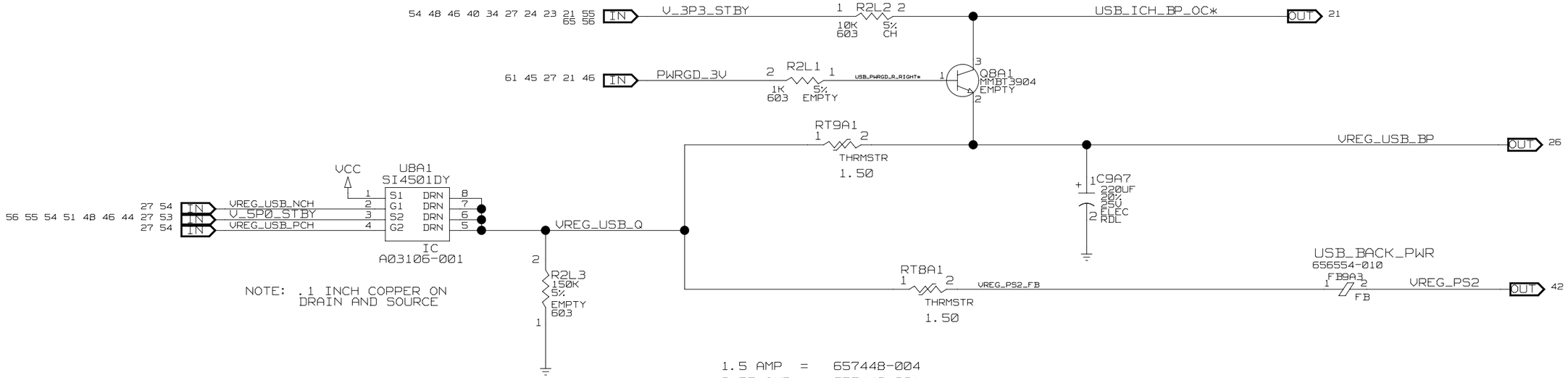
C5V1 1 2 .047UF 20% 50V EMPTY 603 "X7R" (+/- 10%)

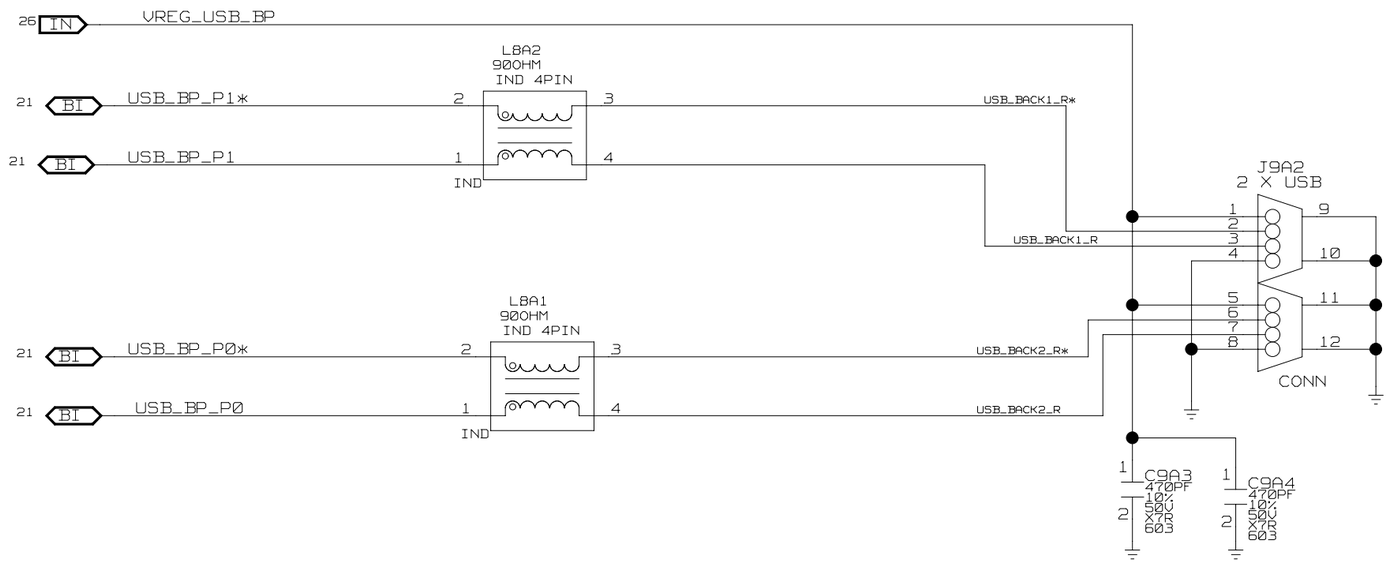
CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN

DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

IDE CONNECTORS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.25 Wed Apr 13 15:32:54 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	25	C3





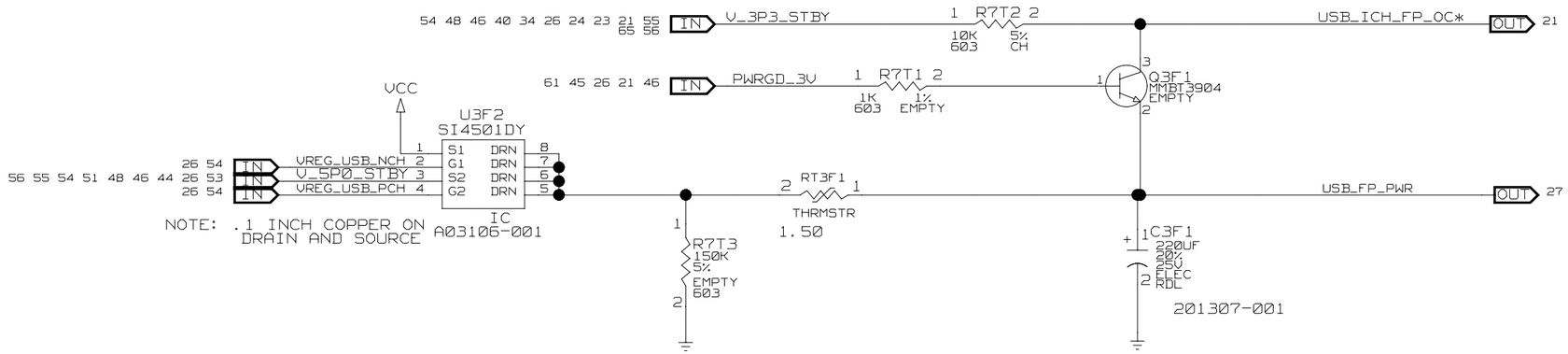
CAD NOTE:
PLACE NEAR USB CONN

USB BACK PANEL & PS/2

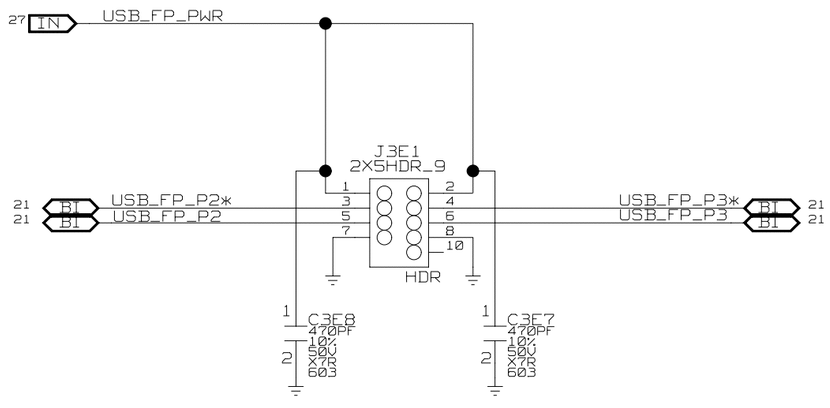
DRAWING
855GMEFB.SCH_1.26
Wed Apr 13 15:32:55 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5200 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	26	C3

FRONT PANEL USB POWER

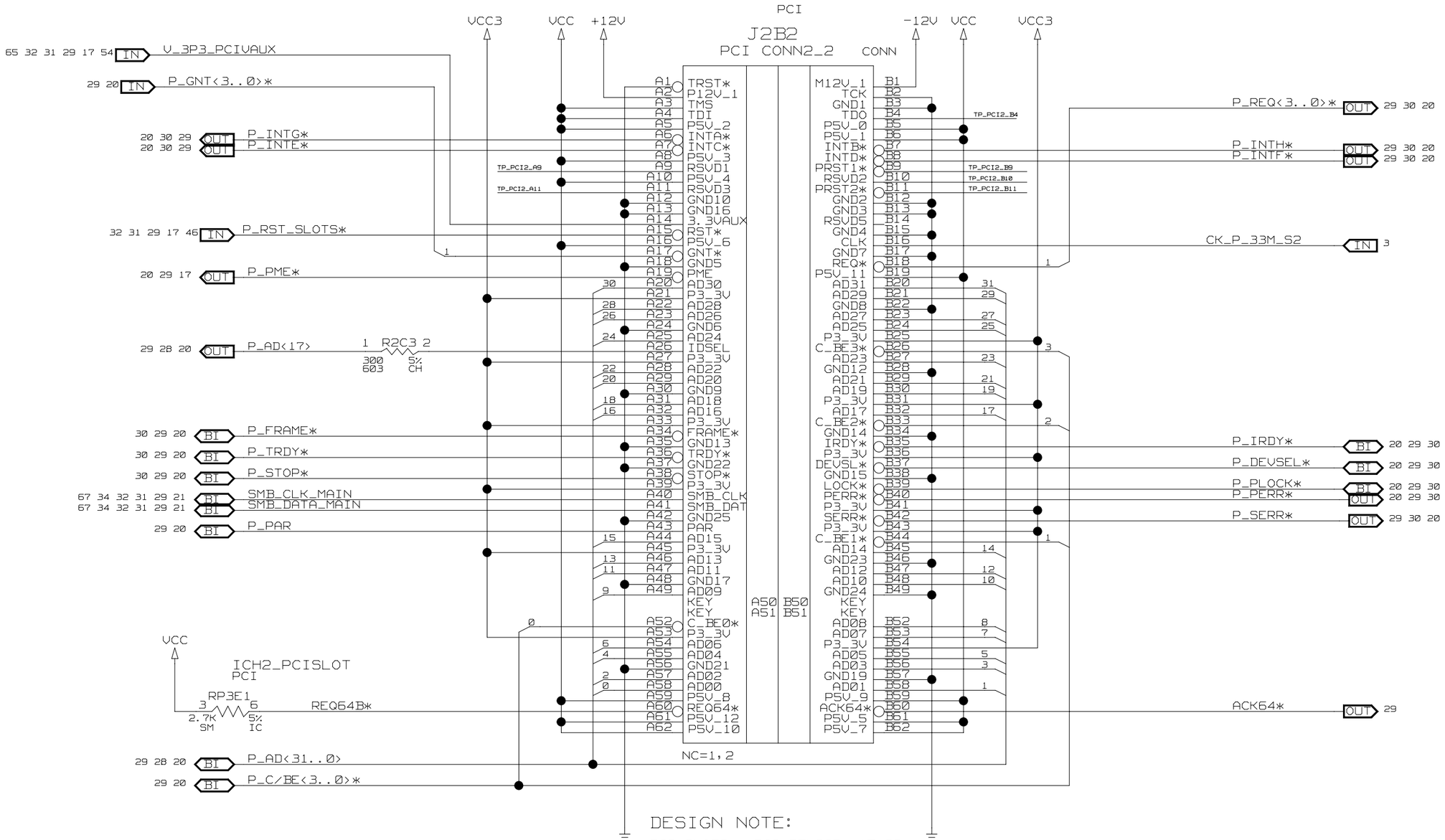


CAD NOTE;
TRACE ROUTING IS 7.5 MIL, 7.5 MIL SPACING



USB FRONT PANEL

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.27 Wed Apr 13 15:32:55 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	27	C3


PCI
J2B2
PCI CONN2_2
CONN
VCC3
VCC
+12V
-12V
V_3P3_PCIVAUX
P_GNT<3..0>*
P_INTG*
P_INTE*
P_RST_SLOTS*
P_PME*
P_AD<17>
R2C3 2
300
603
5%
CH
P_FRAME*
P_TRDY*
P_STOP*
SMB_CLK_MAIN
SMB_DATA_MAIN
P_PAR
TP_PCI2_A9
TP_PCI2_A11
TP_PCI2_B4
TP_PCI2_B9
TP_PCI2_B10
TP_PCI2_B11
P_REQ<3..0>*
P_INTH*
P_INTF*
CK_P_33M_S2
P_IRDY*
P_DEVSEL*
P_PLOCK*
P_PERR*
P_SERR*
ACK64*
REQ64B*
RP3E1
2.7K
SM
5%
IC
ICH2_PCISLOT
PCI
P_AD<31..0>
P_C/BE<3..0>*
NC=1,2
A1 TRST* B1
A2 P12V_1 B2 TCK
A3 TMS B3 GND1
A4 TDI B4 TDO
A5 P5V_2 B5 P5V_0
A6 INTA* B6 P5V_1
A7 INTC* B7 INTB*
A8 P5V_3 B8 INTD*
A9 RSVD1 B9 PRST1*
A10 P5V_4 B10 RSVD2
A11 RSVD3 B11 PRST2*
A12 GND10 B12 GND2
A13 GND16 B13 GND3
A14 3.3VAUX B14 RSVD5
A15 RST* B15 GND4
A16 P5V_6 B16 CLK
A17 GNT* B17 GND7
A18 GND5 B18 REQ*
A19 PME B19 P5V_11
A20 AD30 B20 AD31
A21 P3_3V B21 AD29
A22 AD28 B22 GND8
A23 AD26 B23 AD27
A24 GND6 B24 AD25
A25 AD24 B25 P3_3V
A26 IDSEL B26 C_BE3*
A27 P3_3V B27 AD23
A28 AD22 B28 GND12
A29 AD20 B29 AD21
A30 GND9 B30 AD19
A31 AD18 B31 P3_3V
A32 AD16 B32 AD17
A33 P3_3V B33 C_BE2*
A34 FRAME* B34 GND14
A35 GND13 B35 IRDY*
A36 TRDY* B36 P3_3V
A37 GND22 B37 DEVSL*
A38 STOP* B38 GND15
A39 P3_3V B39 LOCK*
A40 SMB_CLK B40 PERR*
A41 SMB_DAT B41 P3_3V
A42 GND25 B42 SERR*
A43 PAR B43 P3_3V
A44 AD15 B44 C_BE1*
A45 P3_3V B45 AD14
A46 AD13 B46 GND23
A47 AD11 B47 AD12
A48 GND17 B48 AD10
A49 AD09 B49 GND24
KEY A50 B50 KEY
KEY A51 B51 KEY
A52 C_BE0* B52 AD08
A53 P3_3V B53 AD07
A54 AD06 B54 P3_3V
A55 AD04 B55 AD05
A56 GND21 B56 AD03
A57 AD02 B57 GND19
A58 AD00 B58 AD01
A59 P5V_8 B59 P5V_9
A60 REQ64* B60 ACK64*
A61 P5V_12 B61 P5V_5
A62 P5V_10 B62 P5V_7
DESIGN NOTE:
PCI SLOT2 = PCI DEVICE #17/22
REQ/GNT PAIR = #1
IRQ MAP A : B : C : D
G : F : E : H
PCI SLOT 2
DRAWING
855GMEFB.SCH_1.28
Wed Apr 13 15:32:56 2005
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
DOCUMENT NUMBER
30117601
PAGE
28
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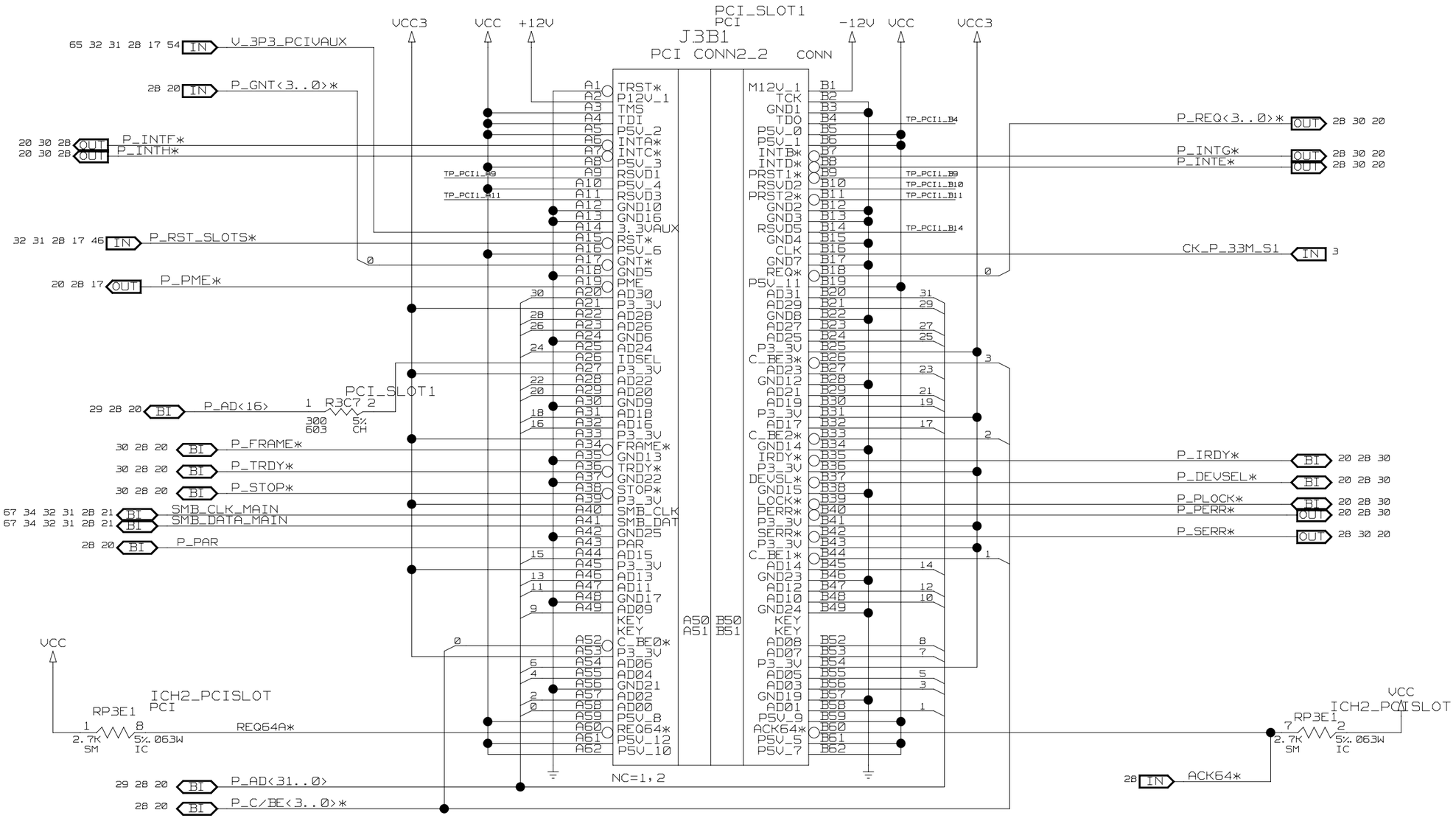
C3



DESIGN NOTE:

PCI SLOT1 = PCI DEVICE #16
REQ/GNT PAIR = #0
IRQ MAP A : B : C : D
F : G : H : E

CLOSEST TO AGP

PCI SLOT 1

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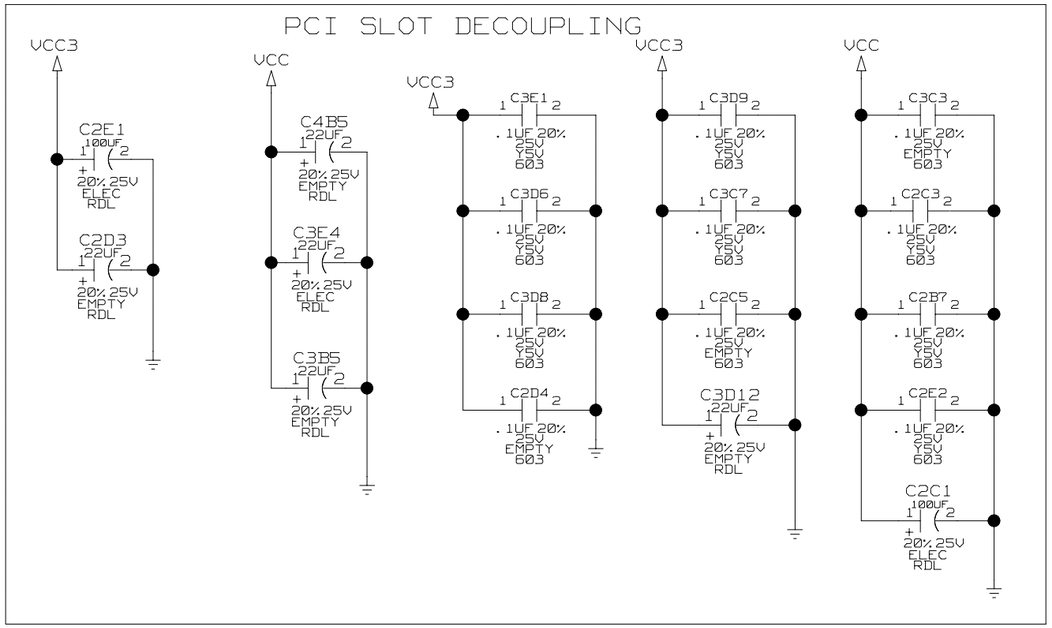
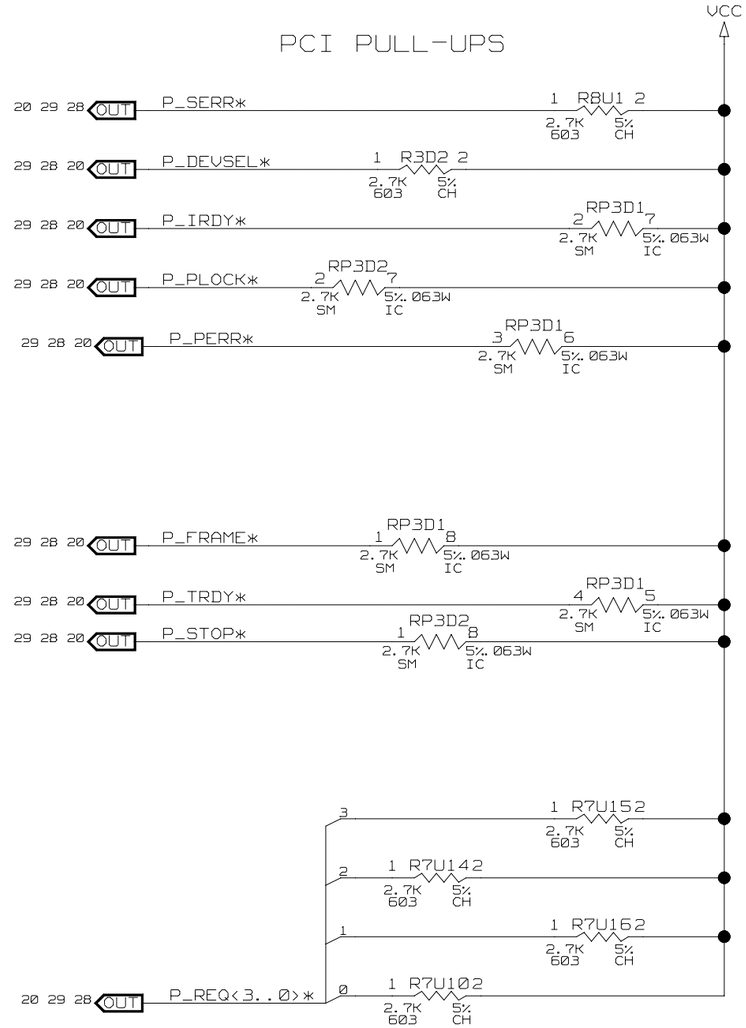
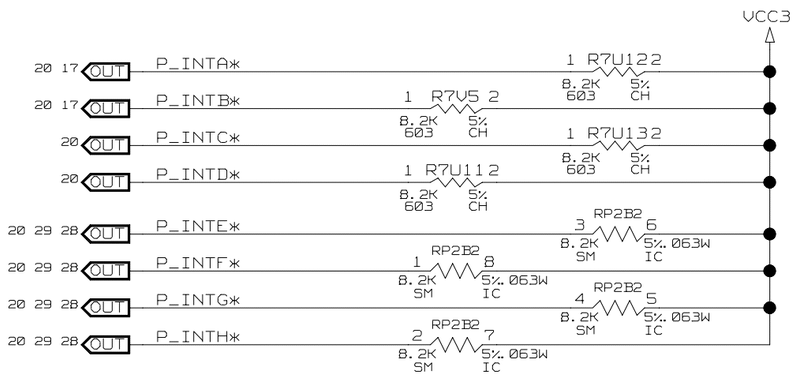
855GMEFB.SCH_1.29 Wed Apr 13 15:32:56 2005	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 29	REV C3

PCI SLOT DECOUPLING

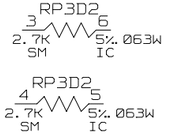


PCI PULL-UPS





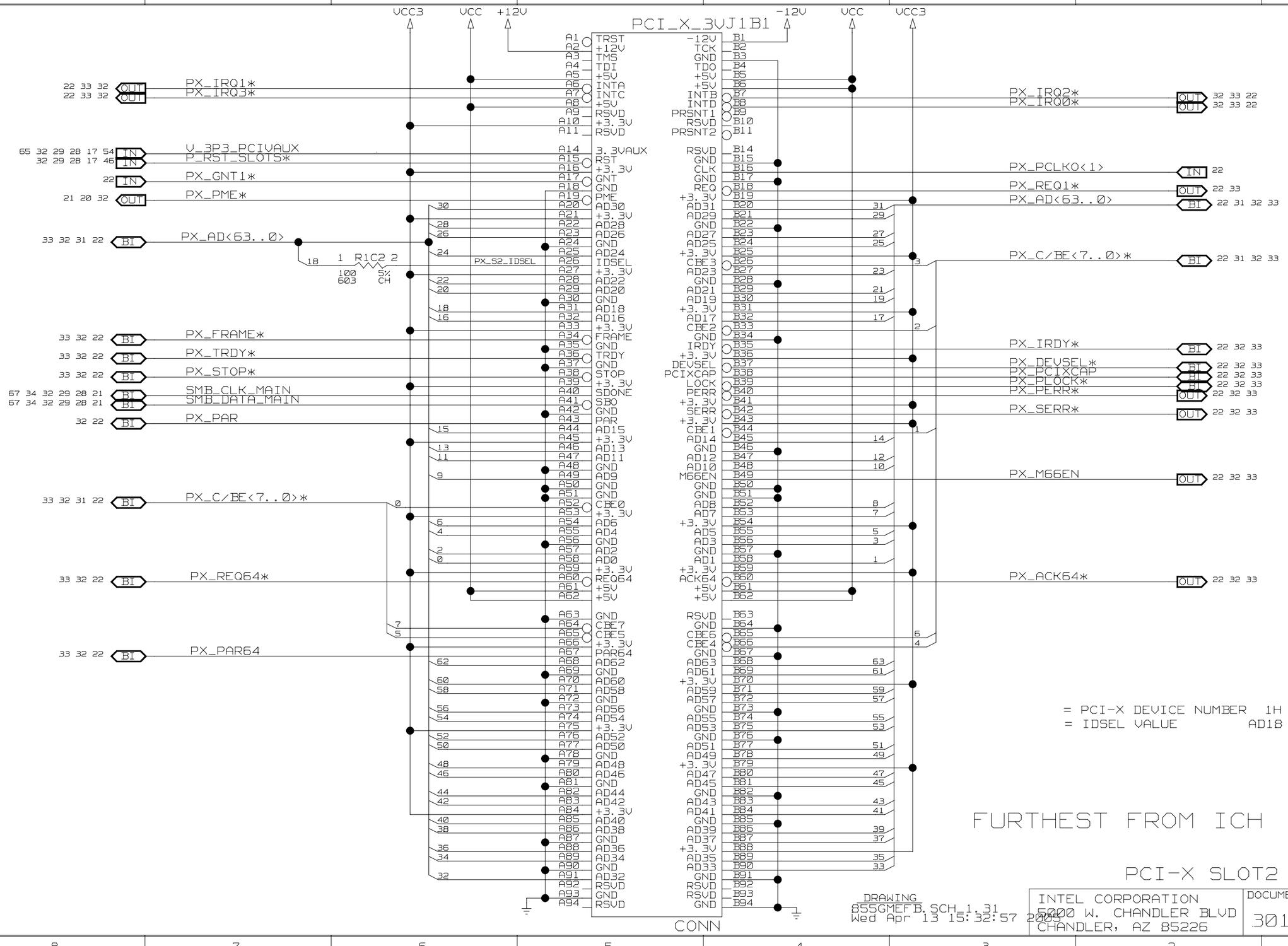
SPARE SECTIONS



PCI TERMINATION AND DECOUPLING

DRAWING
855GMEFB.SCH_1.30
Wed Apr 13 15:32:57 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	30	C3


PCI_X_3VJ1B1
VCC3
VCC
+12V
-12V
PX_IRQ1*
PX_IRQ3*
V_3P3_PCIVAUX
P_RST_SLOTS*
PX_GNT1*
PX_PME*
PX_AD<63..0>
R1C2 2
100
603
5%
CH
PX_S2_IDSEL
PX_FRAME*
PX_TRDY*
PX_STOP*
SMB_CLK_MAIN
SMB_DATA_MAIN
PX_PAR
PX_C/BE<7..0>*
PX_REQ64*
PX_PAR64
PX_IRQ2*
PX_IRQ0*
PX_PCLKO<1>
PX_REQ1*
PX_AD<63..0>
PX_C/BE<7..0>*
PX_IRDY*
PX_DEVSEL*
PX_PCIXCAP
PX_PLOCK*
PX_PERR*
PX_SERR*
PX_M66EN
PX_ACK64*
= PCI-X DEVICE NUMBER 1H
= IDSEL VALUE AD18
FURTHEST FROM ICH
PCI-X SLOT2
CONN
DRAWING
855GMEFB.SCH.1.31
Wed Apr 13 15:32:57 2005
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
DOCUMENT NUMBER
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PAGE
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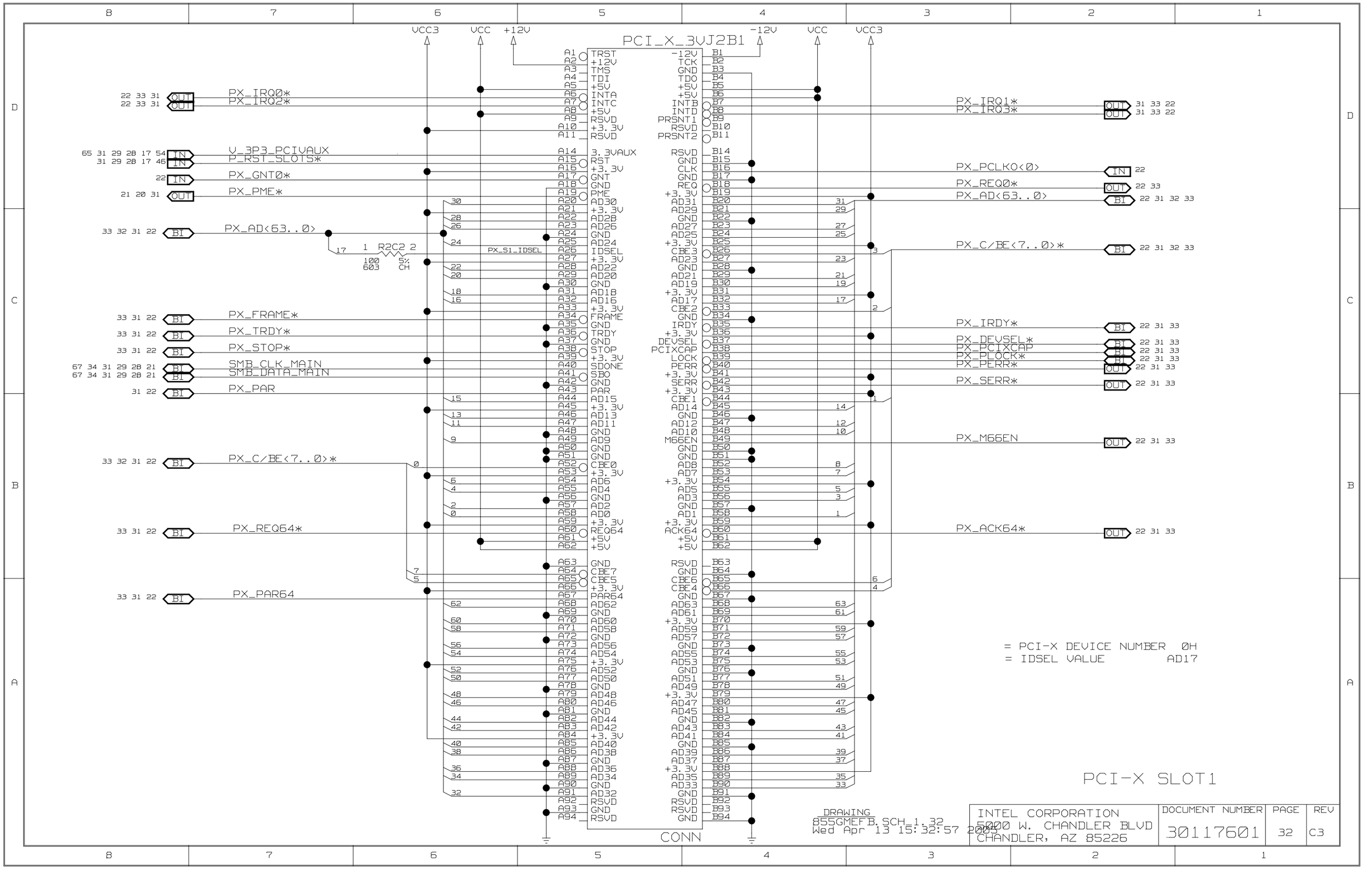
REV
C3


PCI_X_3VJ2B1
VCC3
VCC
+12V
-12V
PX_IRQ0*
PX_IRQ2*
PX_IRQ1*
PX_IRQ3*
V_3P3_PCIVAUX
P_RST_SLOTS*
PX_PCLKO<0>
PX_GNT0*
PX_REQ0*
PX_PME*
PX_AD<63..0>
PX_AD<63..0>
PX_S1_IDSEL
R2C2
100
603
5%
CH
PX_C/BE<7..0>*
PX_FRAME*
PX_IRDY*
PX_TRDY*
PX_DEVSEL*
PX_STOP*
PX_PCIXCAP
PX_PLOCK*
SMB_CLK_MAIN
SMB_DATA_MAIN
PX_PERR*
PX_PAR
PX_SERR*
PX_M66EN
PX_C/BE<7..0>*
PX_REQ64*
PX_ACK64*
PX_PAR64
= PCI-X DEVICE NUMBER 0H
= IDSEL VALUE AD17
PCI-X SLOT1
CONN
DRAWING
855GMEFB.SCH_1.32
Wed Apr 13 15:32:57 2005
INTEL CORPORATION
5000 W. CHANDLER BLVD
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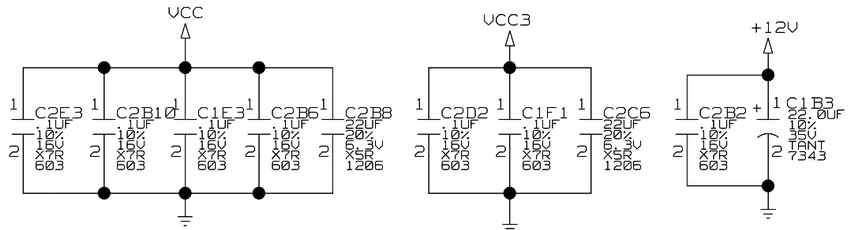
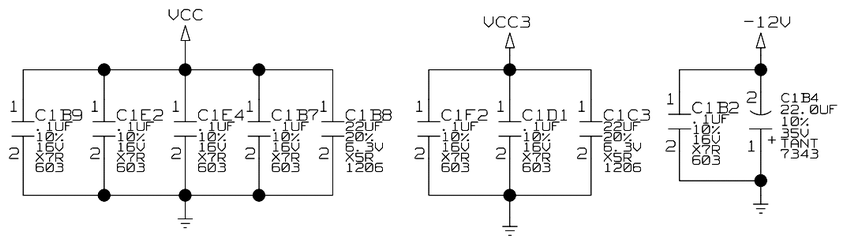
C3

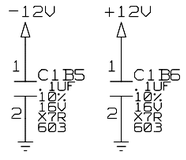
PCI-X SLOT 1 DECOUPLING

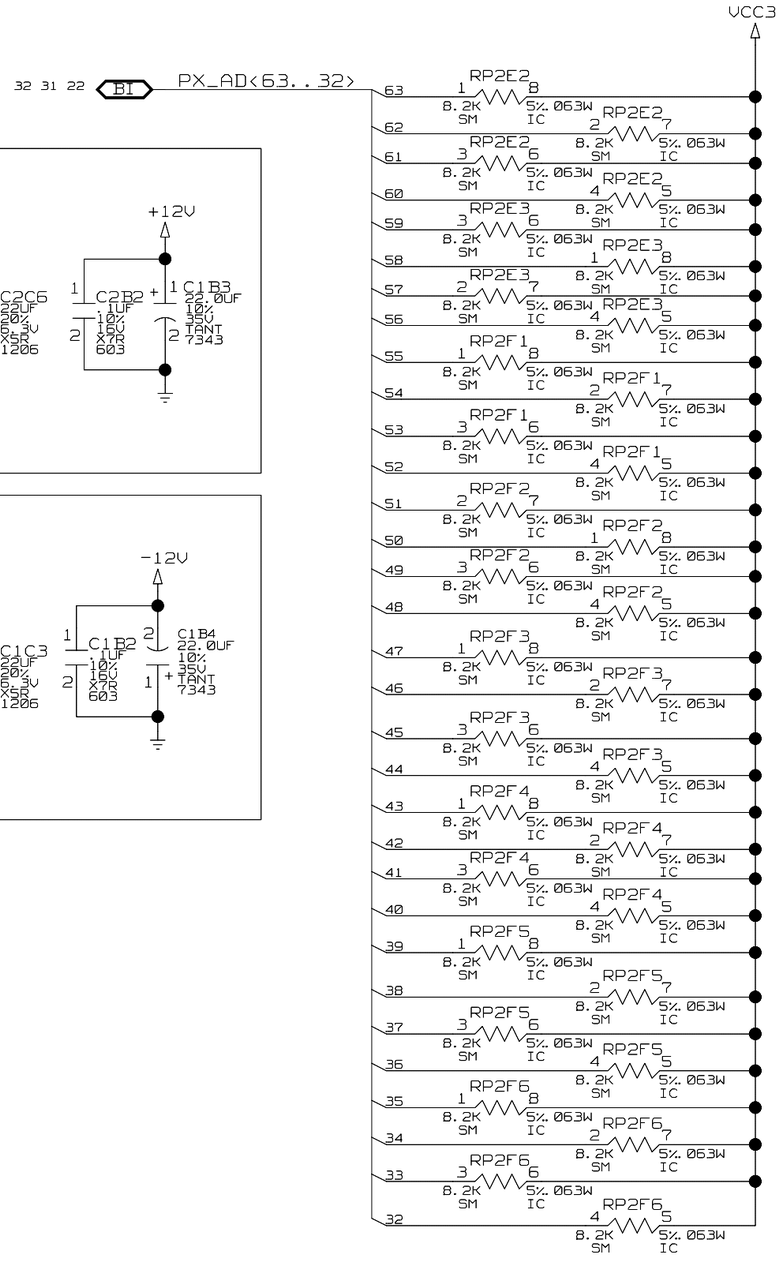


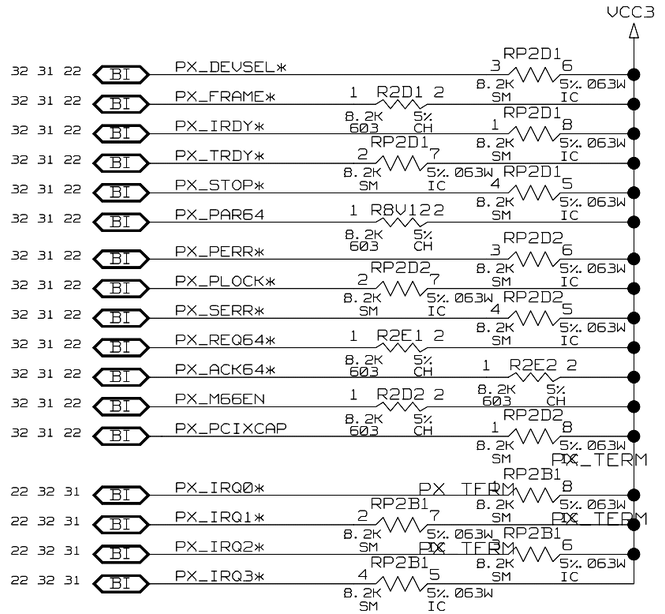
PCI-X SLOT 2 DECOUPLING

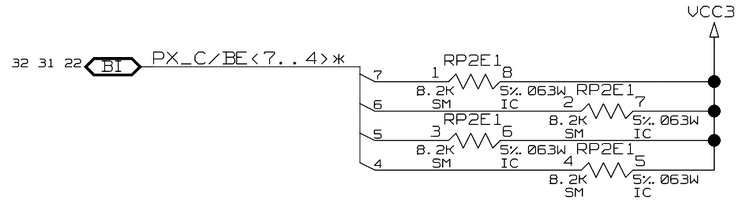


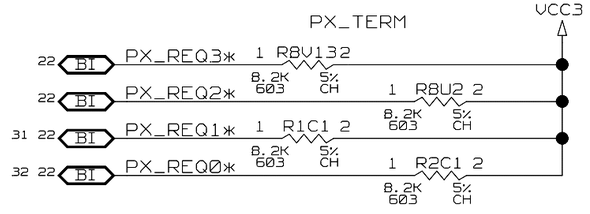
PCI-X SHARED DECOUPLING





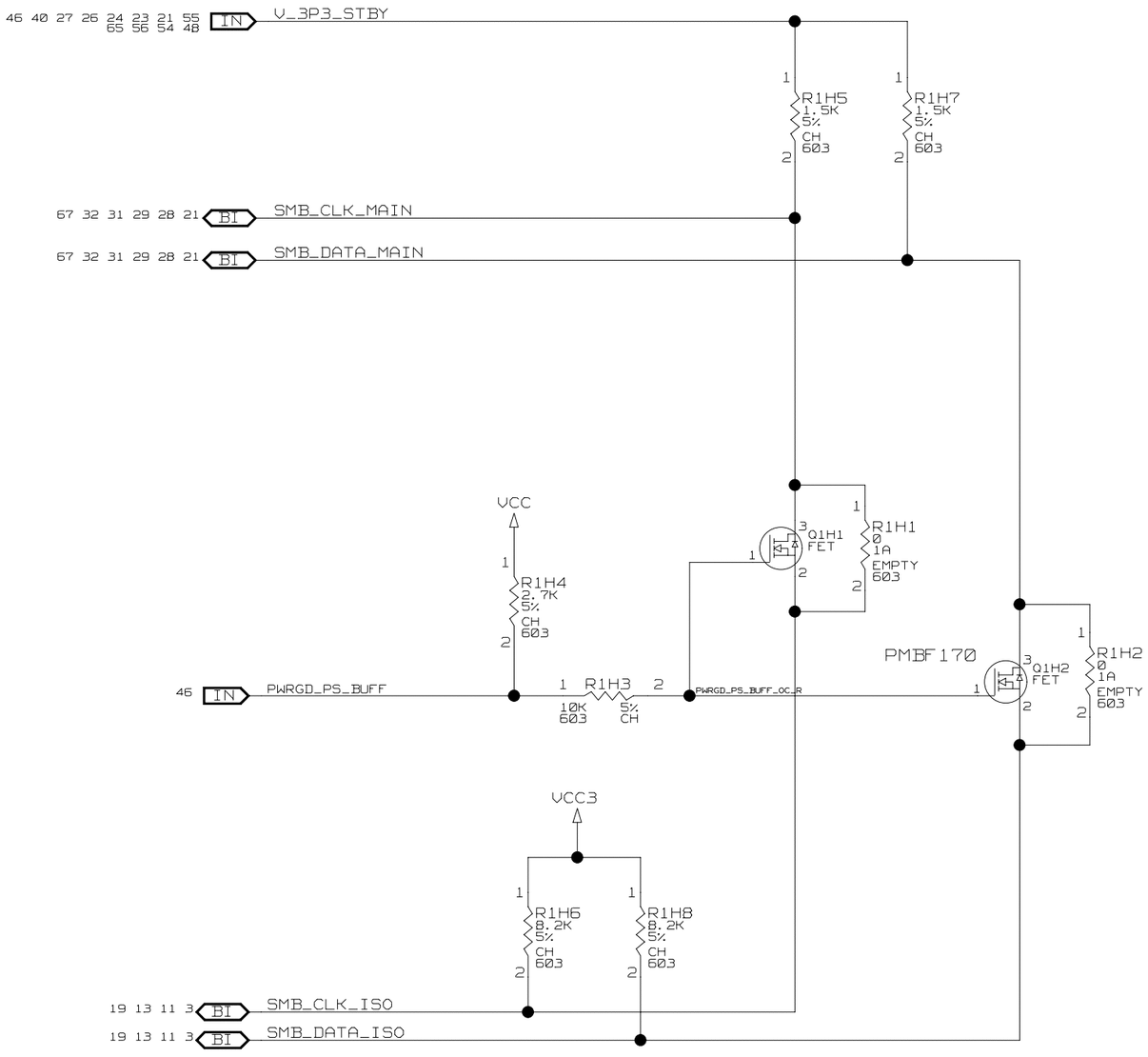


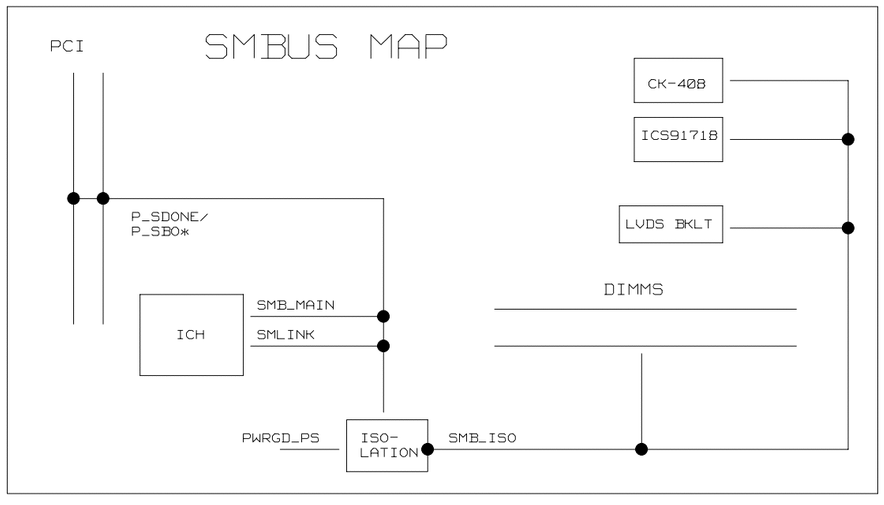




PCI-X TERMINATION

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.33 Wed Apr 13 15:32:58 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	33	C3



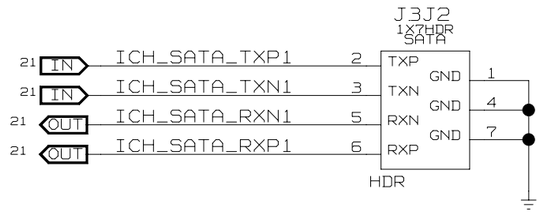


SMBUS ISOLATION CIRCUIT

DRAWING
855GMEFB.SCH.1.34
Wed Apr 13 15:32:58 2005

INTEL CORPORATION
5200 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	34	C3

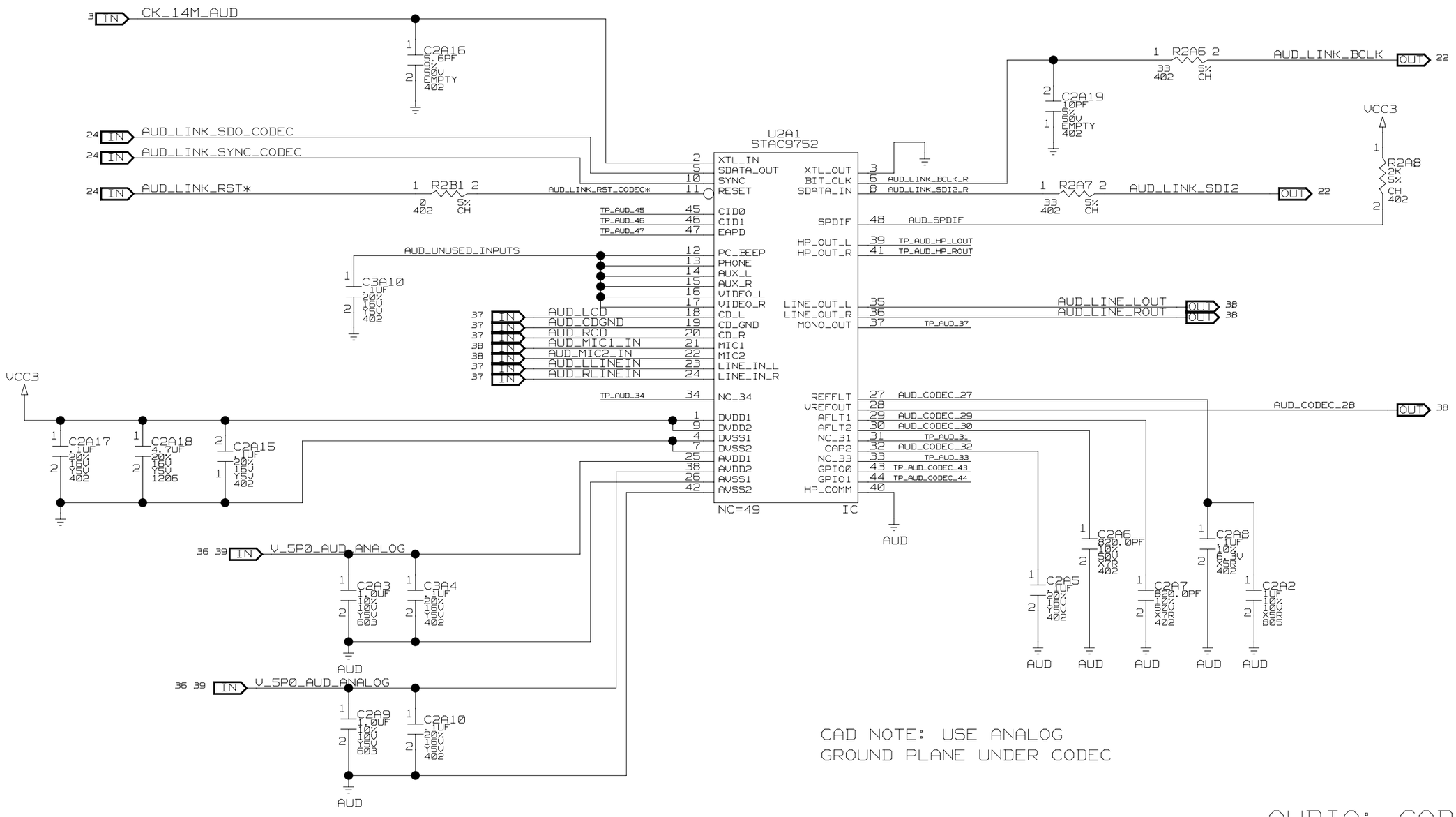


SERIAL ATA CONNECTORS.

DRAWING
855GMEFB.SCH_1.35
Wed Apr 13 15:32:58 2005

INTEL CORPORATION
5200 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	35	C3

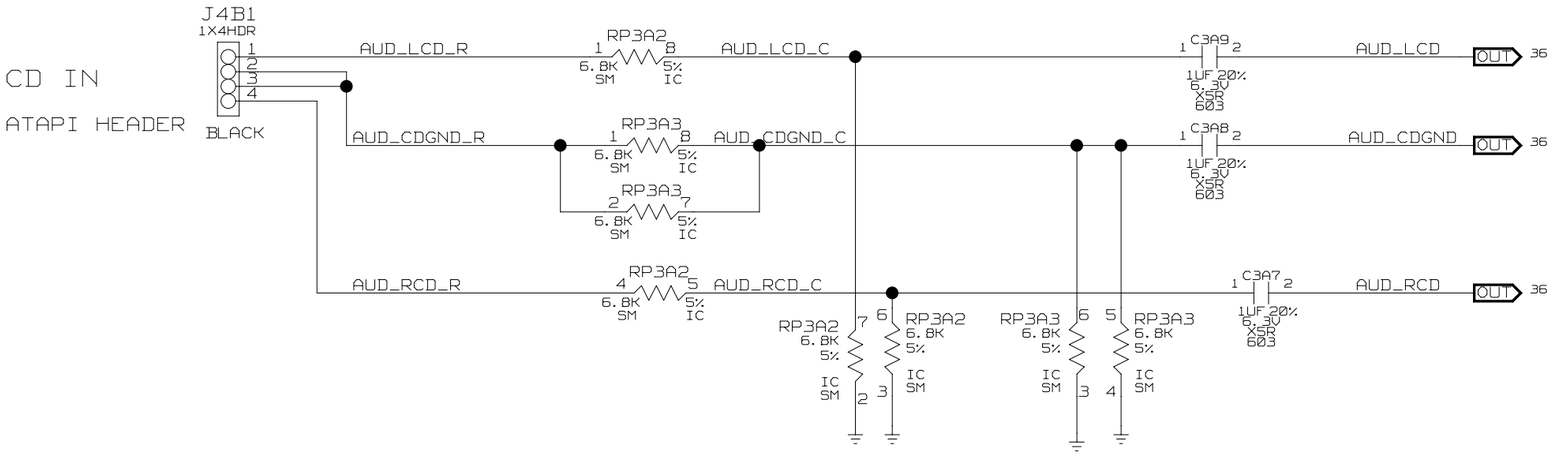


AUDIO: CODEC

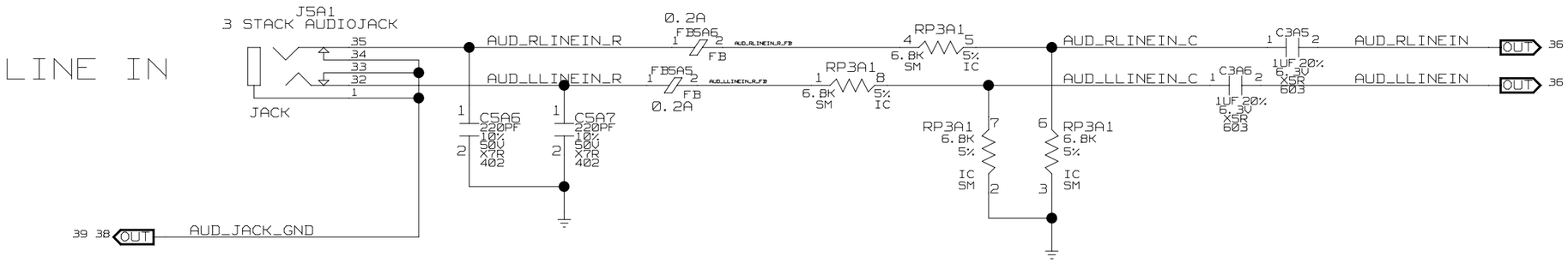
DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.36 Wed Apr 13 15:32:59 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	36	C3

CD IN

ATAPI HEADER



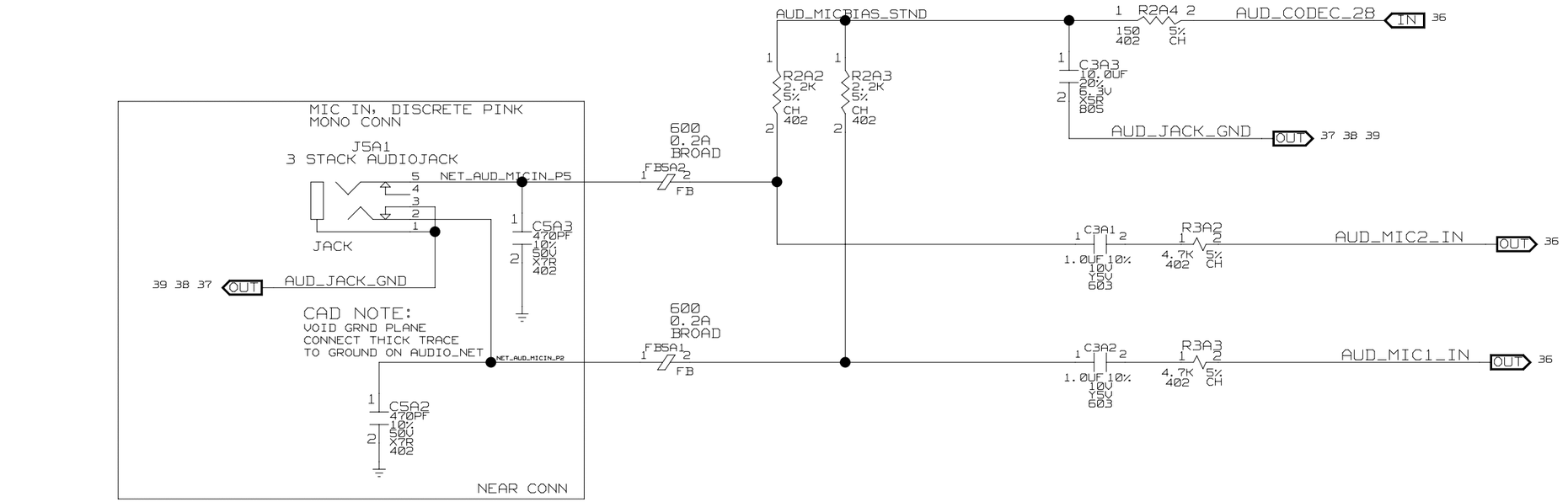
LINE IN



AUDIO: CD IN, LINE IN

DRAWING
855GMEFB.SCH_1.37
Wed Apr 13 15:33:00 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5200 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	37	C3

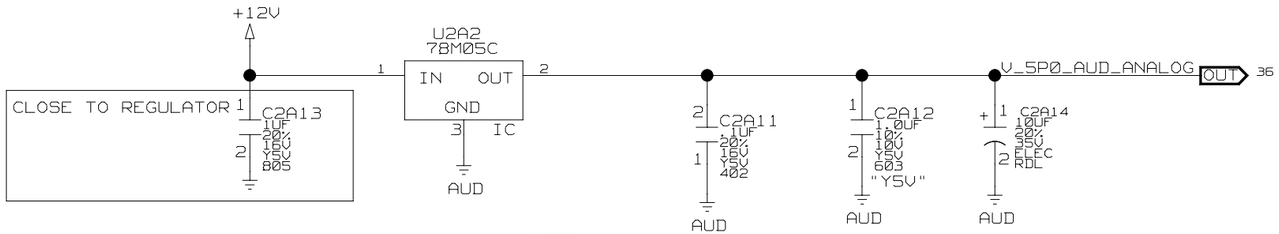


AUDIO: MIC IN, LINEOUT

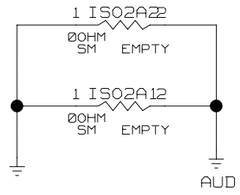
DRAWING
855GMEFB.SCH_1.38
Wed Apr 13 15:33:00 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5200 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	38	C3

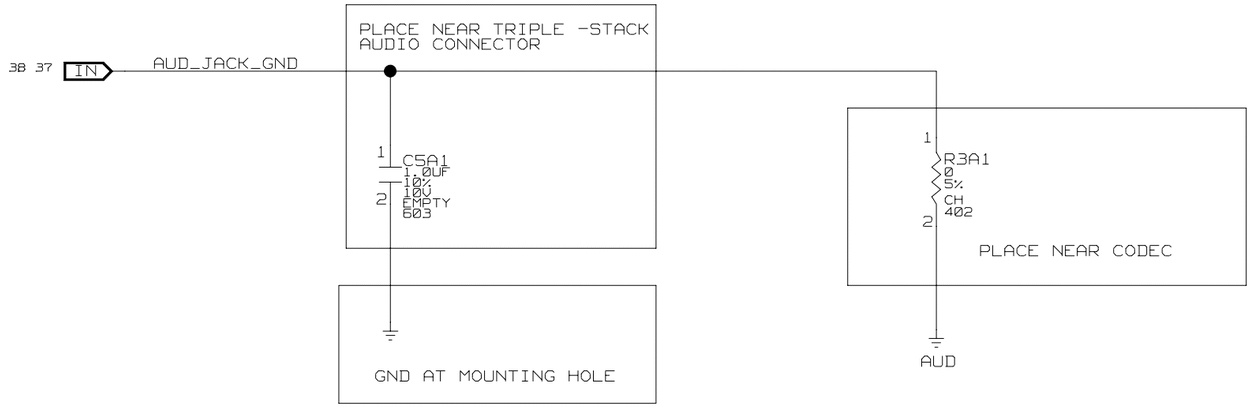
REGULATOR THERMAL TAB SHOULD BE SOLDERED
TO A COPPER PAD THAT IS LARGE ENOUGH
TO ALLOW 5 TO 10 GROUND VIAS AROUND
THE COMPONENT FOR COOLING



NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO
CAPS AND THEN THROUGH SEVERAL
VIAS TO V_5P0_AUD_ANALOG

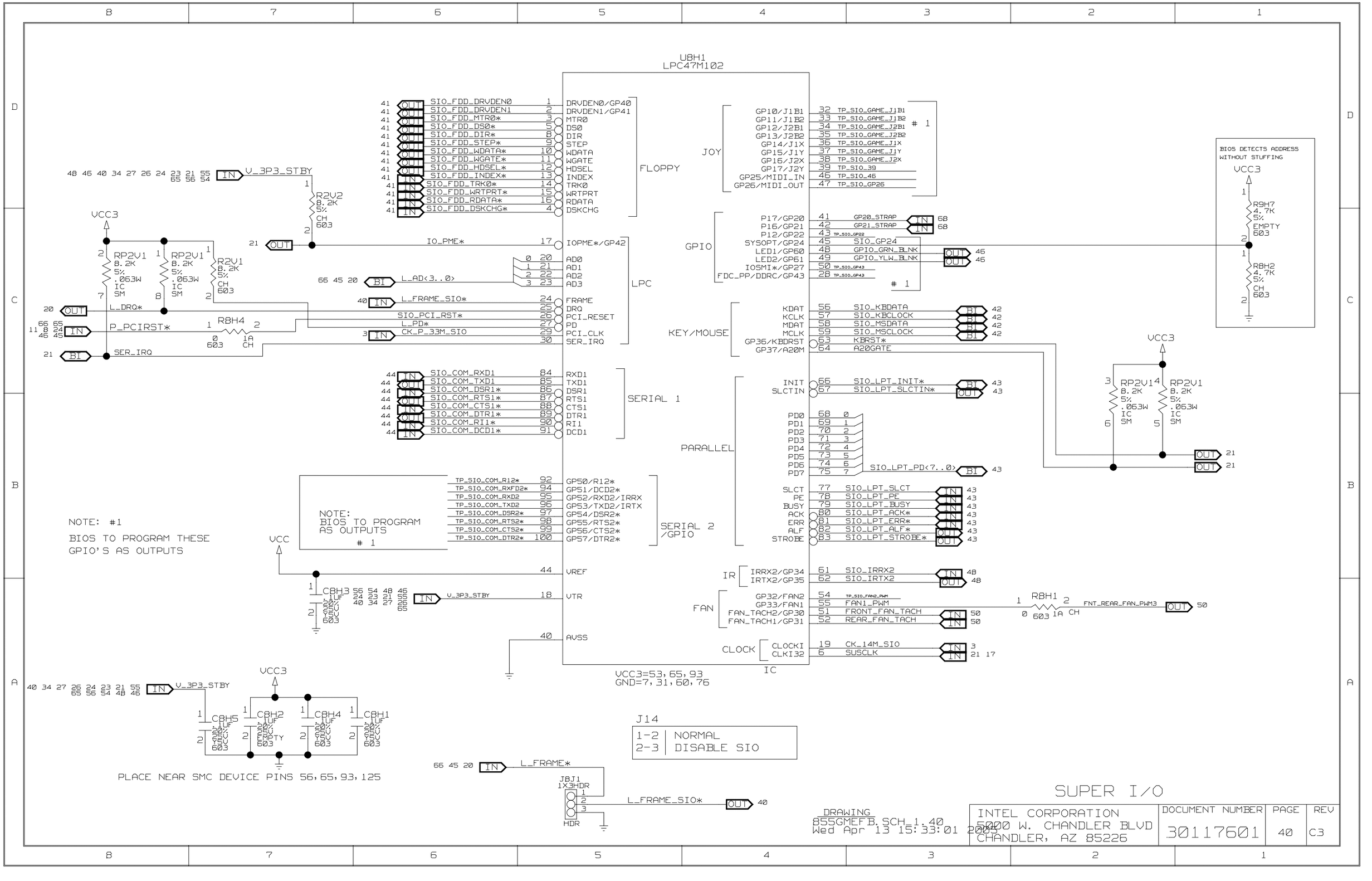


OVERLAPPING PADS
GROUND ISOLATION SYMBOL



AUDIO: VREG

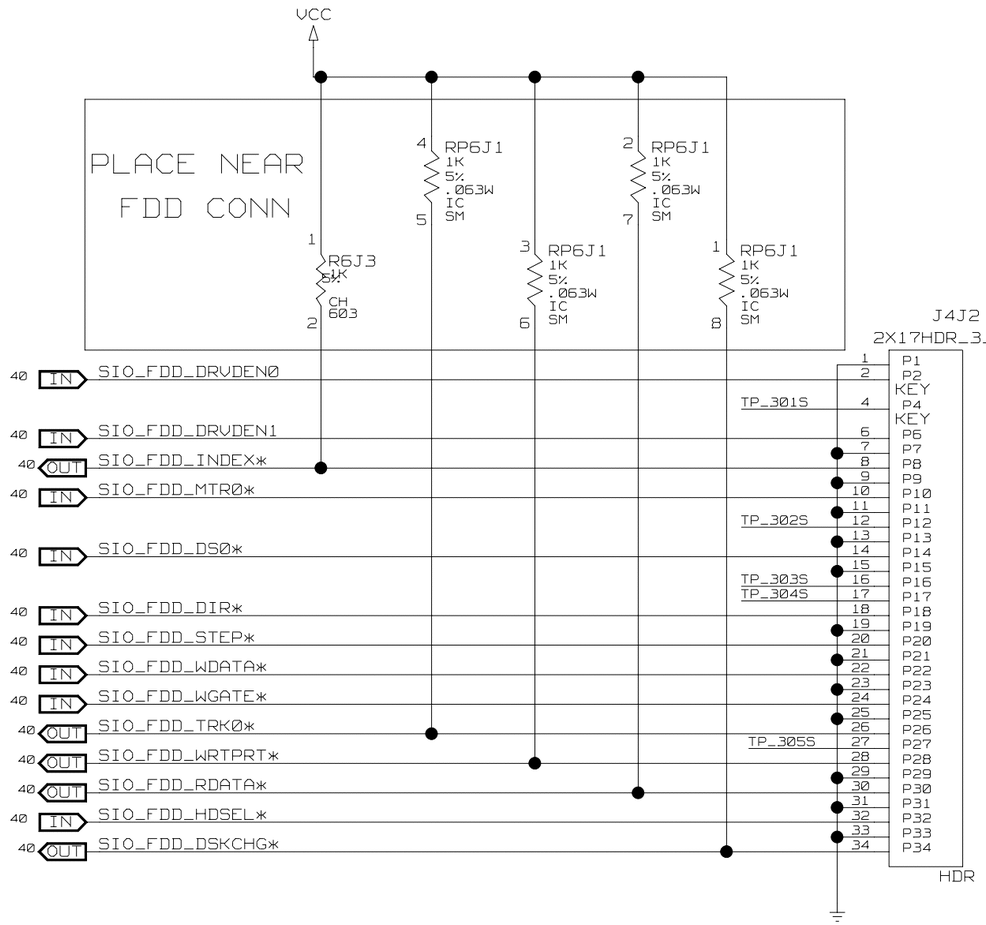
DRAWING				
855GMEFB.SCH.1.39 Wed Apr 13 15:33:00 2005	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 39	REV C3



SUPER I/O

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 40	REV C3

DRAWING
855GMEFB.SCH_1.40
Wed Apr 13 15:33:01 2005

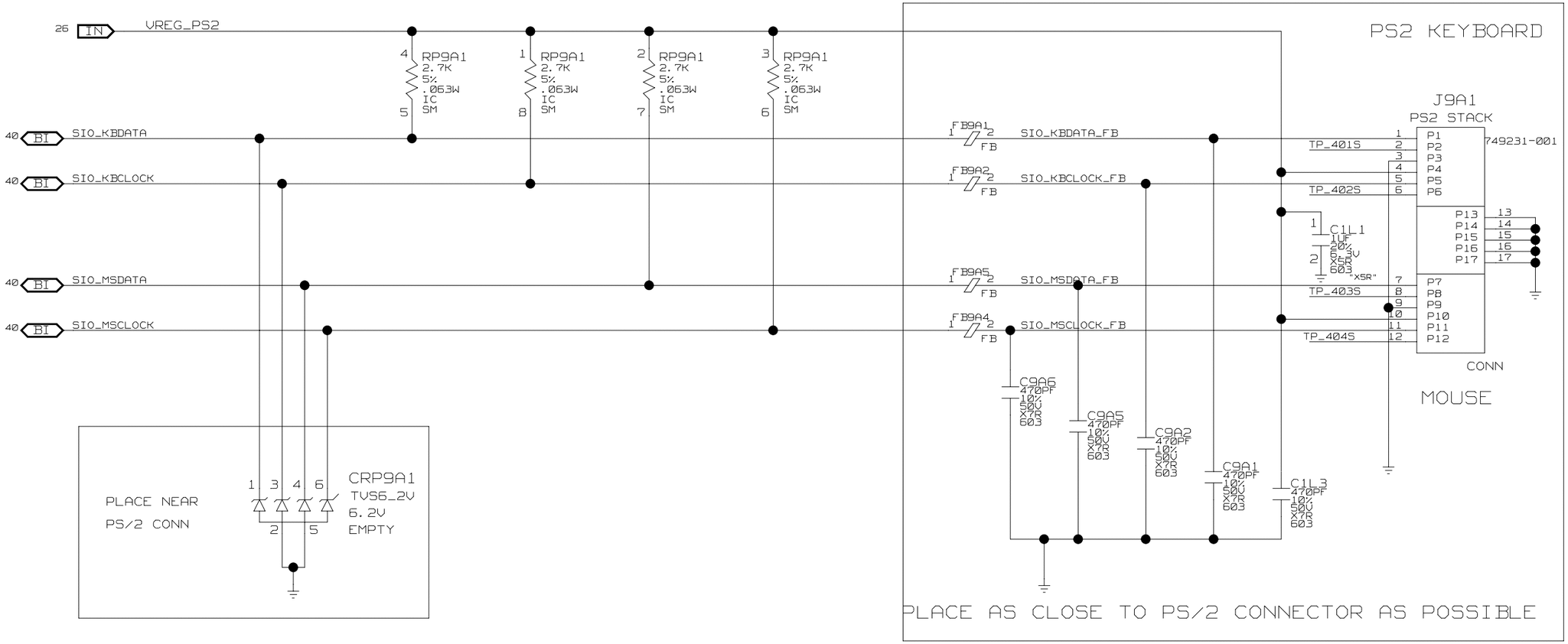


FLOPPY CONNECTOR

DRAWING
855GMEFB.SCH.1.41
Wed Apr 13 15:33:01 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	41	C3

COMPONENTS ARE DFM29



ATX DOUBLE-STACKED

PS/2 STACK

DRAWING				
855GMEFB.SCH_1.42 Wed Apr 13 15:33:01 2005	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 42	REV C3

COMPONENTS ARE DFM29

40 IN SIO_LPT_PD<7..0>

RP7A3 6 SIO_LPT_PD6_R
RP7A3 5 SIO_LPT_PD7_R
RP7A2 7 SIO_LPT_PD0_R
RP7A2 8 SIO_LPT_PD1_R
RP7A2 5 SIO_LPT_PD2_R
RP7A2 6 SIO_LPT_PD3_R
RP7A3 7 SIO_LPT_PD4_R
RP7A3 8 SIO_LPT_PD5_R
33 SM, 5%. 063W IC

VCC

RP7A4 2.7K 5% .063W IC SM

40 IN SIO_LPT_STROBE* RP7A5 7 SIO_LPT_STROBE_R*
40 IN SIO_LPT_ALF* RP7A5 8 SIO_LPT_ALF_R*
40 IN SIO_LPT_INIT* RP7A5 5 SIO_LPT_INIT_R*
40 IN SIO_LPT_SLCTIN* RP7A5 6 SIO_LPT_SLCTIN_R*
33 SM, 5%. 063W IC

VCC

RP8A1 10K 5% .063W IC SM
R7A2 10K 5% CH 603

40 OUT SIO_LPT_ACK*
40 OUT SIO_LPT_BUSY
40 OUT SIO_LPT_PE
40 OUT SIO_LPT_SLCT
40 OUT SIO_LPT_ERR*

PLACE NEAR
LPT CONN

C8A5 C8A4 C8A3 C8A2 C8A1 C7A15 C7A14 C7A13 C7A12 C7A11 C7A10 C7A9 C7A8 C7A7 C7A6 C7A5
220PF 10% 50V X7R 603

J7A2
TALL DSUB 25
749179-001
1 14 2 15 3 16 4 17 5 18 6 19 7 20 8 21 9 22 10 23 11 24 12 25 13
DSUB
GND=26, 27, 28

PARALLEL PORT

DRAWING
855GMEFB.SCH_1.43
Wed Apr 13 15:33:02 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	43	C3

DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N

SERIAL PORT A

U6B1
GD75232S

SIO_COM_DCD1* (OUT) → RY1 (19) → RA1 (2)
SIO_COM_DSR1* (OUT) → RY2 (18) → RA2 (3)
SIO_COM_RXD1 (OUT) → RY3 (17) → RA3 (4)
SIO_COM_CTS1* (OUT) → RY4 (14) → RA4 (7)
SIO_COM_RI1* (OUT) → RY5 (12) → RA5 (9)
SIO_COM_RTS1* (IN) → DA1 (16) → DY1 (5)
SIO_COM_TXD1 (IN) → DA2 (15) → DY2 (6)
SIO_COM_DTR1* (IN) → DA3 (13) → DY3 (8)
VDD+ (1) → +12V
VDD- (10) → -12V

NOTE DIRECTION IC

VCC=20
GND=11
VCC=VCC

C6B4 470PF 10% 50V X7R 603
C6A10 470PF 10% 50V X7R 603
C6B3 470PF 10% 50V X7R 603
C6A8 470PF 10% 50V X7R 603
C6A7 470PF 10% 50V X7R 603
C6A9 470PF 10% 50V X7R 603
C6B2 470PF 10% 50V X7R 603
C6B1 470PF 10% 50V X7R 603

J6B1
SERIAL PORT
2X5HDR_10

SIO_COM_DCD1_232 → P1
SIO_COM_RXD1_232* → P2
SIO_COM_TXD1_232* → P3
SIO_COM_DTR1_232 → P4
P5
SIO_COM_DSR1_232 → P6
SIO_COM_RTS1_232 → P7
SIO_COM_CTS1_232 → P8
SIO_COM_RI1_232 → P9
KEY

HDR

SERIAL PORT B

U8A2
GD75232S

ICH_COM_DCD0* (OUT) → RY1 (19) → RA1 (2)
ICH_COM_DSR0* (OUT) → RY2 (18) → RA2 (3)
ICH_COM_RXD0 (OUT) → RY3 (17) → RA3 (4)
ICH_COM_CTS0* (OUT) → RY4 (14) → RA4 (7)
ICH_COM_RI0* (OUT) → RY5 (12) → RA5 (9)
ICH_COM_RTS0* (IN) → DA1 (16) → DY1 (5)
ICH_COM_TXD0 (IN) → DA2 (15) → DY2 (6)
ICH_COM_DTR0* (IN) → DA3 (13) → DY3 (8)
VDD+ (1) → +12V
VDD- (10) → -12V

NOTE DIRECTION IC

VCC=20
GND=11

C2L1 470PF 10% 50V X7R 603
C2L2 470PF 10% 50V X7R 603
C2L3 470PF 10% 50V X7R 603
C2L6 470PF 10% 50V X7R 603
C3L1 470PF 10% 50V X7R 603
C2L4 470PF 10% 50V X7R 603
C2L5 470PF 10% 50V X7R 603
C2L7 470PF 10% 50V X7R 603

J8A1
2 ROW
DSUB

ICH_COM_DCD0_232 → 1
ICH_COM_DSR0_232 → 6
ICH_COM_RXD0_232* → 2
ICH_COM_RTS0_232 → 7
ICH_COM_TXD0_232* → 3
ICH_COM_CTS0_232 → 8
ICH_COM_DTR0_232 → 4
ICH_COM_RI0_232 → 9
5
10
11

U6A1
GD75232S

ICH_COM_DCD1* (OUT) → RY1 (19) → RA1 (2)
ICH_COM_DSR1* (OUT) → RY2 (18) → RA2 (3)
ICH_COM_RXD1 (OUT) → RY3 (17) → RA3 (4)
ICH_COM_CTS1* (OUT) → RY4 (14) → RA4 (7)
ICH_COM_RI1* (OUT) → RY5 (12) → RA5 (9)
ICH_COM_RTS1* (IN) → DA1 (16) → DY1 (5)
ICH_COM_TXD1 (IN) → DA2 (15) → DY2 (6)
ICH_COM_DTR1* (IN) → DA3 (13) → DY3 (8)
VDD+ (1) → +12V
VDD- (10) → -12V

NOTE DIRECTION IC

VCC=20
GND=11

C4L1 470PF 10% 50V X7R 603
C4L2 470PF 10% 50V X7R 603
C4L3 470PF 10% 50V X7R 603
C4L6 470PF 10% 50V X7R 603
C4L8 470PF 10% 50V X7R 603
C4L4 470PF 10% 50V X7R 603
C4L5 470PF 10% 50V X7R 603
C4L7 470PF 10% 50V X7R 603

J6A1
2 ROW
DSUB

ICH_COM_DCD1_232 → 1
ICH_COM_DSR1_232 → 6
ICH_COM_RXD1_232* → 2
ICH_COM_RTS1_232 → 7
ICH_COM_TXD1_232* → 3
ICH_COM_CTS1_232 → 8
ICH_COM_DTR1_232 → 4
ICH_COM_RI1_232 → 9
5
10
11

+12V
C4M1 1UF 20% 25V Y5V 603
C6A2 1UF 20% 25V Y5V 603
C2M2 1UF 20% 25V Y5V 603

-12V
C4L9 1UF 20% 25V Y5V 603
C6A1 1UF 20% 25V Y5V 603
C2M1 1UF 20% 25V Y5V 603

V_5P0_STBY (IN) 53 26 27 46 48 51 54 55 56
C4M2 1UF 20% 25V Y5V 603

VCC
C6A5 1UF 20% 25V Y5V 603
C2M3 1UF 20% 25V Y5V 603

PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY

SERIAL PORTS

DRAWING
855GMEFB.SCH_1.44
Wed Apr 13 15:33:02 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
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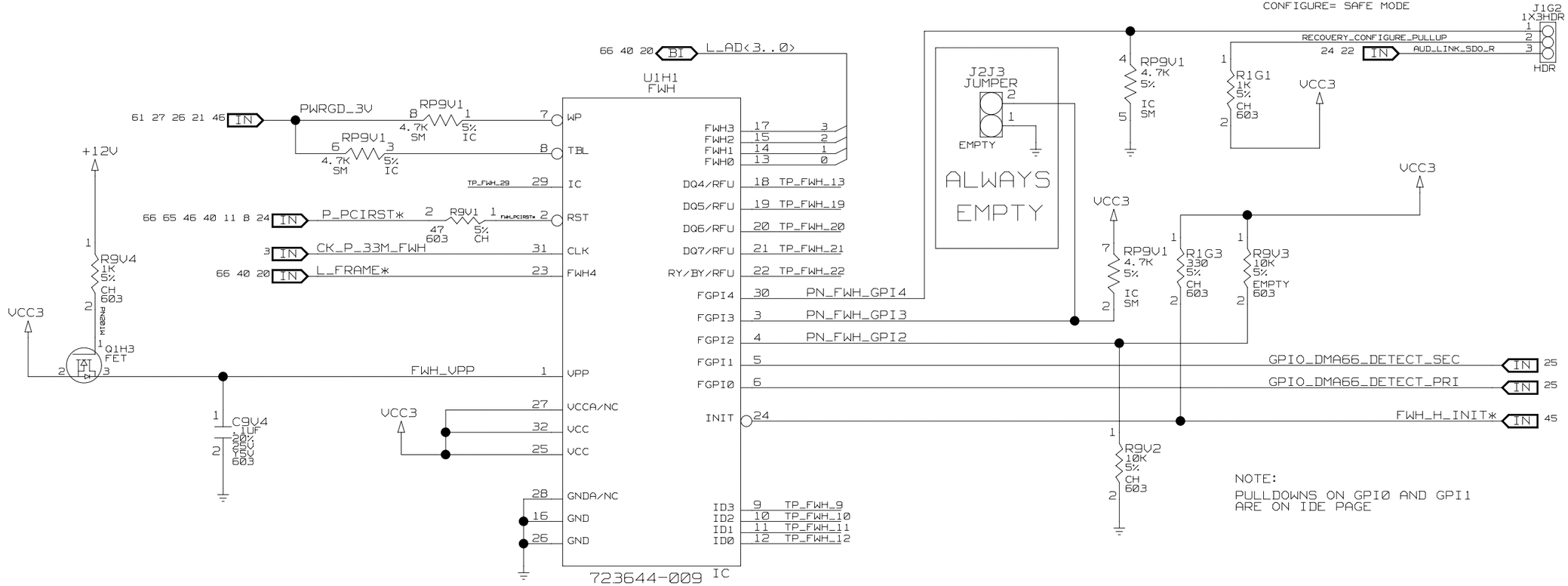
RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

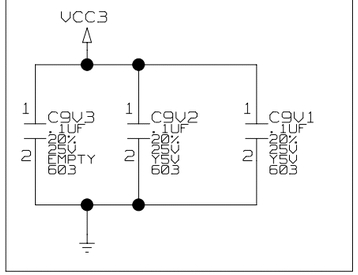


NOTE:
PULLDOWNS ON GPI0 AND GPI1 ARE ON IDE PAGE

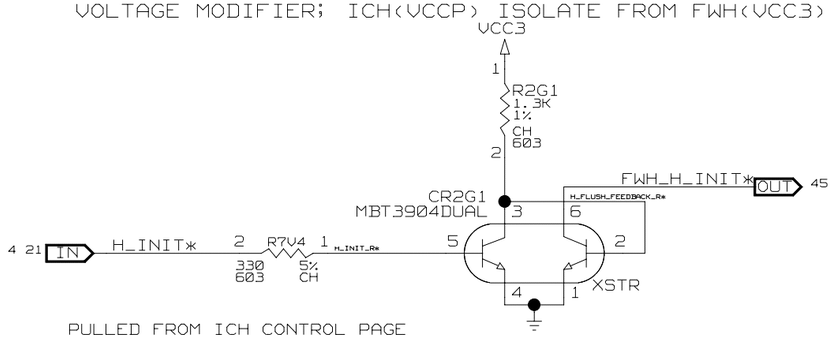
FWH SOCKET - INTEL P/N: 201138-032, AMP P/N: 822475-1

PLCC EXTRACTION TOOL
AMP: 821980-1 OR
AMP: 822476-1

FIRMWARE HUB DECOUPLING



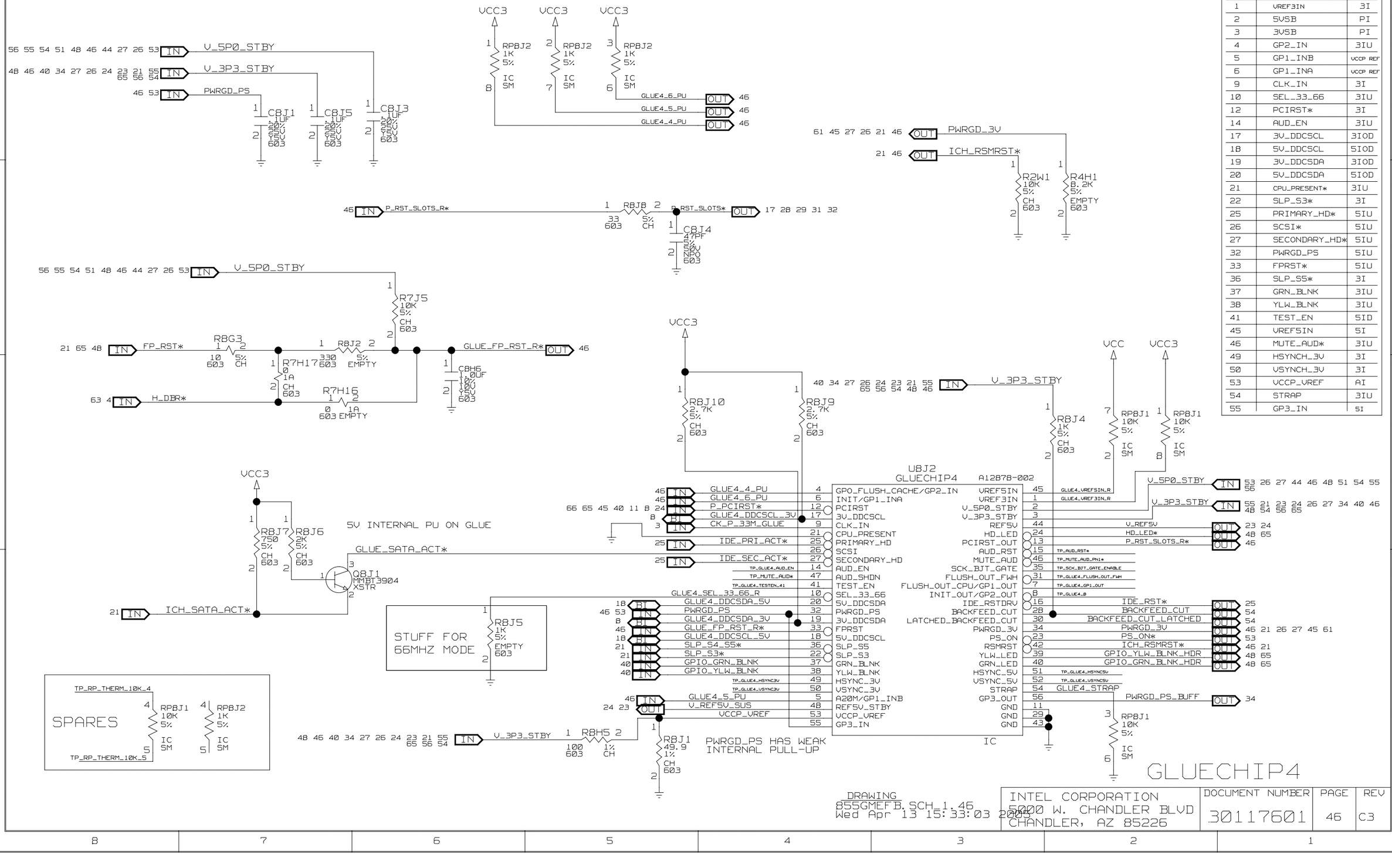
VOLTAGE MODIFIER; ICH(VCCP) ISOLATE FROM FWH(VCC3)



PULLED FROM ICH CONTROL PAGE

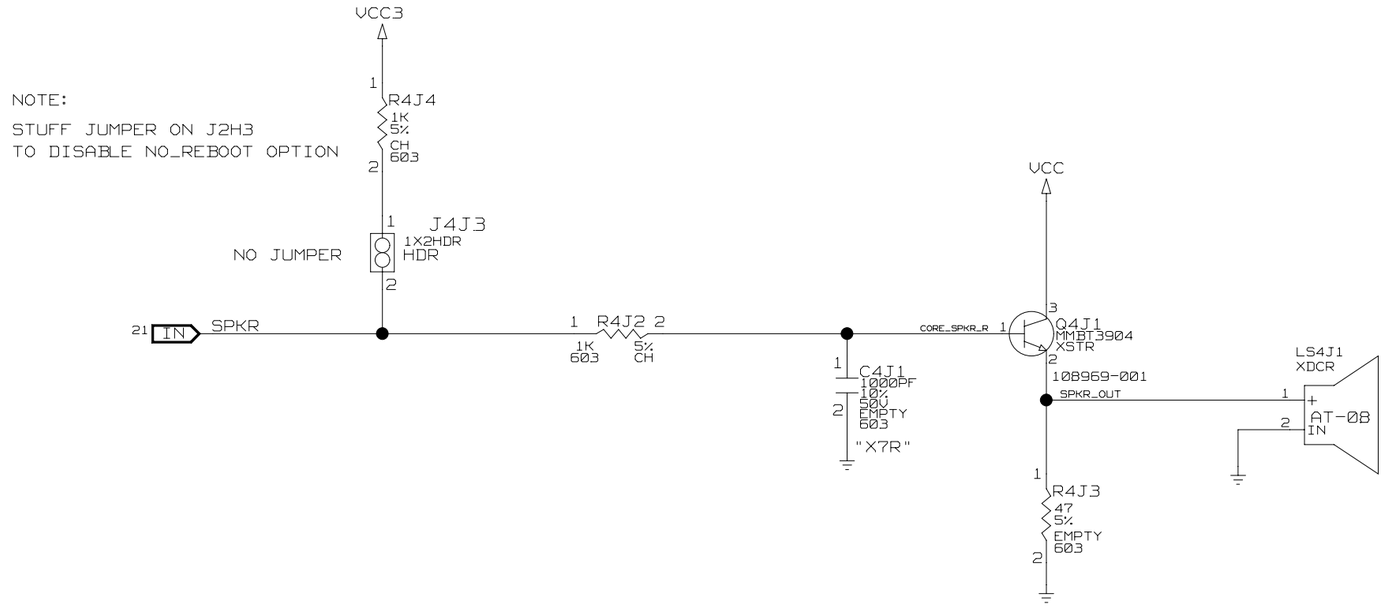
FIRMWARE HUB

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.45 Wed Apr 13 15:33:03 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	45	C3


GLUE4 INPUTS
PIN FUNCTION TYPE
1 VREF3IN 3I
2 5VSB PI
3 3VSB PI
4 GP2_IN 3IU
5 GP1_INB VCCP REF
6 GP1_INA VCCP REF
9 CLK_IN 3I
10 SEL_33_66 3IU
12 PCIRST* 3I
14 AUD_EN 3IU
17 3V_DDCSCL 3IOD
18 5V_DDCSCL 5IOD
19 3V_DDCSDA 3IOD
20 5V_DDCSDA 5IOD
21 CPU_PRESENT* 3IU
22 SLP_S3* 3I
25 PRIMARY_HD* 5IU
26 SCSI* 5IU
27 SECONDARY_HD* 5IU
32 PWRGD_PS 5IU
33 FPRST* 5IU
36 SLP_S5* 3I
37 GRN_BLNK 3IU
38 YLW_BLNK 3IU
41 TEST_EN 5ID
45 VREF5IN 5I
46 MUTE_AUD* 3IU
49 HSYNCH_3V 3I
50 VSYNCH_3V 3I
53 VCCP_VREF AI
54 STRAP 3IU
55 GP3_IN 5I
V_5P0_STBY
V_3P3_STBY
PWRGD_PS
C8J1 .1UF
C8J5 .1UF
C8J3 .1UF
VCC3
RP8J2 1K
GLUE4_6_PU
GLUE4_5_PU
GLUE4_4_PU
PWRGD_3V
ICH_RSMRST*
R2W1 10K
R4H1 8.2K
P_RST_SLOTS_R*
R8J8 33
C8J4 47PF
P_RST_SLOTS*
R7J5 10K
FP_RST*
R8G3 10
R8J2 330
GLUE_FP_RST_R*
R7H17 0
C8H6 1.0UF
H_DBR*
R7H16 0
R8J10 2.7K
R8J9 2.7K
R8J4 1K
RP8J1 10K
V_5P0_STBY
V_3P3_STBY
V_REF5V
HD_LED*
P_RST_SLOTS_R*
IDE_RST*
BACKFEED_CUT
BACKFEED_CUT_LATCHED
PWRGD_3V
PS_ON*
ICH_RSMRST*
GPIO_YLW_BLNK_HDR
GPIO_GRN_BLNK_HDR
GLUE4_STRAP
PWRGD_PS_BUFF
R8J7 750
R8J6 2K
Q8J1 MMBT3904 XSTR
GLUE_SATA_ACT*
ICH_SATA_ACT*
5V INTERNAL PU ON GLUE
STUFF FOR 66MHZ MODE
R8J5 1K EMPTY
SPARES
TP_RP_THERM_10K_4
TP_RP_THERM_10K_5
RP8J1 10K
RP8J2 1K
R8H5 100
R8J1 49.9
PWRGD_PS HAS WEAK INTERNAL PULL-UP
U8J2
GLUECHIP4
A12878-002
GPO_FLUSH_CACHE/GP2_IN
INIT/GP1_INA
PCIRST
3V_DDCSCL
CLK_IN
CPU_PRESENT
PRIMARY_HD
SCSI
SECONDARY_HD
AUD_EN
AUD_SHDN
TEST_EN
SEL_33_66
5V_DDCSDA
PWRGD_PS
3V_DDCSDA
FPRST
5V_DDCSCL
SLP_S5
SLP_S3
GRN_BLNK
YLW_BLNK
HSYNC_3V
VSYNC_3V
A20M/GP1_INB
REF5V_STBY
VCCP_VREF
GP3_IN
VREF5IN
VREF3IN
V_5P0_STBY
V_3P3_STBY
REF5V
HD_LED
PCIRST_OUT
AUD_RST
MUTE_AUD
SCK_BJT_GATE
FLUSH_OUT_FWH
FLUSH_OUT_CPU/GP1_OUT
INIT_OUT/GP2_OUT
IDE_RSTDRV
BACKFEED_CUT
LATCHED_BACKFEED_CUT
PWRGD_3V
PS_ON
RSMRST
YLW_LED
GRN_LED
HSYNC_5V
VSYNC_5V
STRAP
GP3_OUT
GND
IC
GLUECHIP4
DRAWING
855GMEFB.SCH_1.46
Wed Apr 13 15:33:03 2005
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
DOCUMENT NUMBER
30117601
PAGE
46
REV
C3

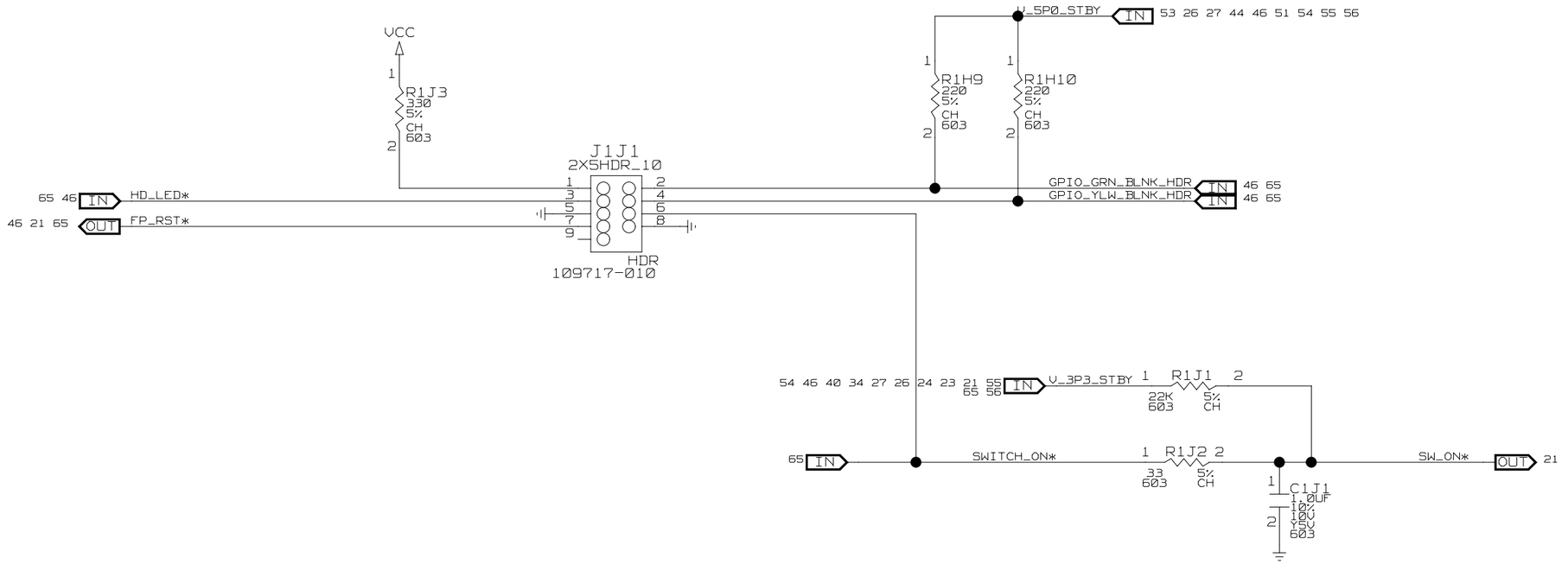
NOTE:

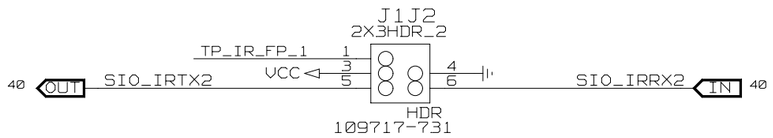
STUFF JUMPER ON J2H3
TO DISABLE NO_REBOOT OPTION



SPEAKER

DRAWING		DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.47 Wed Apr 13 15:33:04 2005	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	47	C3





FRONT PANEL HEADER
IR HEADER

DRAWING
855GMEFB.SCH_1.48
Wed Apr 13 15:33:04 2005

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	48	C3

MTG1A1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG5A1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG9B1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG1J1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG9G1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG5J1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG9J1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

CONNECTOR LOCATION

	X	Y
PS/2	8525	6210
USB/LAN	7965	5927
COM	6940	6115
PAR	5362	5843
VGA	5136	6190
DIAGLED	4636	6045
USB	4151	6026
AUD	3291	6218

LABELS

DEBUG
U3B1
SILK
1
INTELtm
'INTEL' LOGO SILKSCREEN
2.0 X 0.250
MAKE EMPTY ON BOM

LB9J1
LABEL
1
A19177-001
1375X250_TARGET

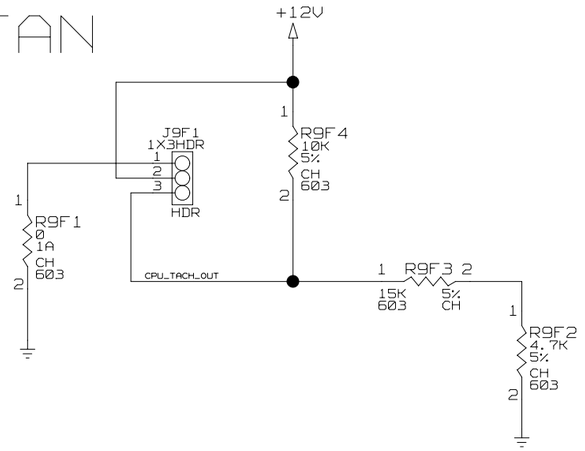
MOUNTING HOLES & LABELS

DRAWING
855GMEFB.SCH_1.49
Wed Apr 13 15:33:04 2005

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

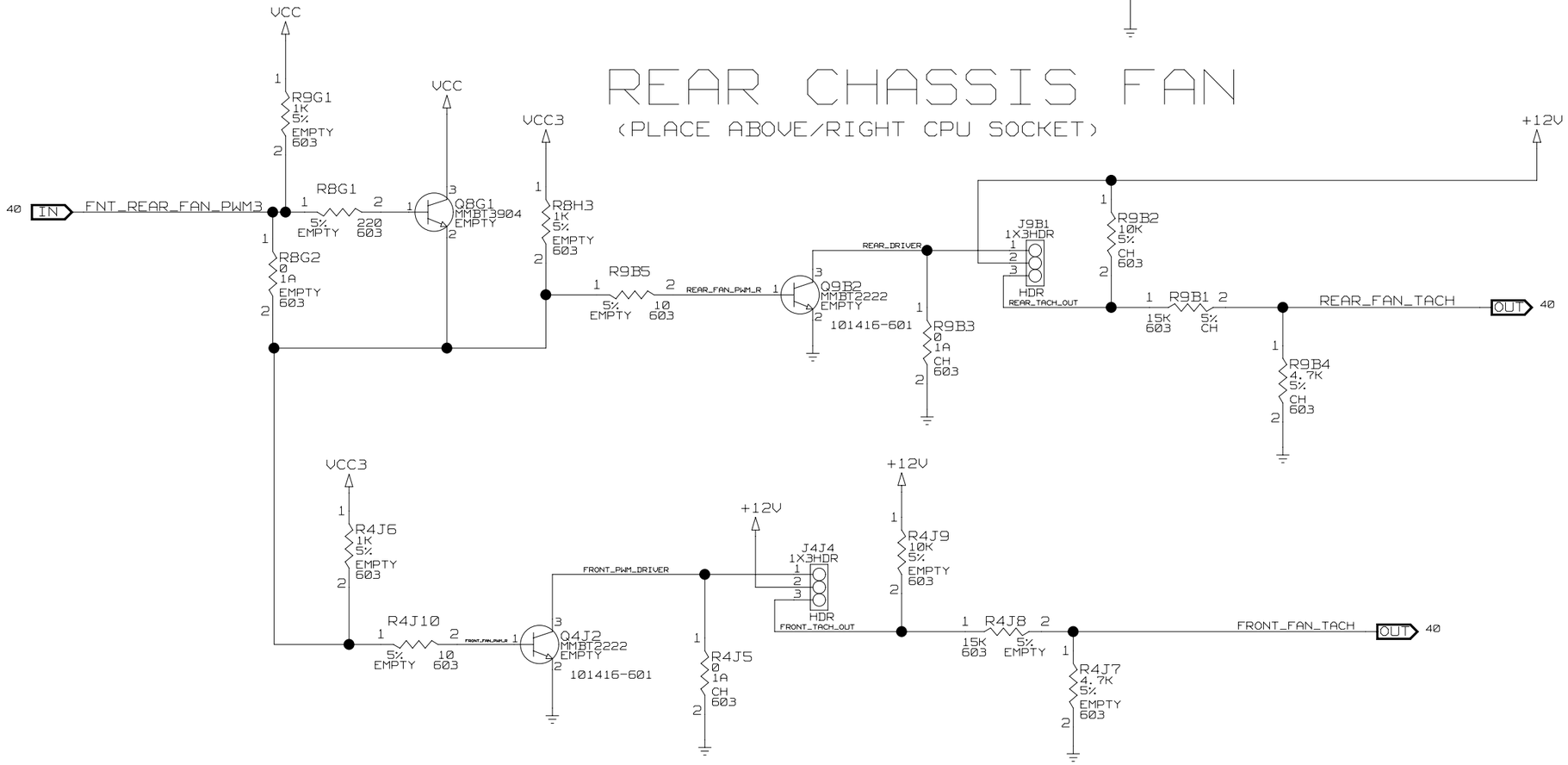
CPU ALWAYS-ON FAN

(PLACE BELOW/RIGHT CPU SOCKET)



REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)



(PLACE LOWER LEFT CORNER OF PLATFORM)

CPU & CHASSIS FANS

DRAWING
855GMEFB.SCH_1.50
Wed Apr 13 15:33:05 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	50	C3

ROOM=DCL_DDR_VR

STUFFING OPTIONS DEPENDING ON CONTROLLER

LOCATION	NCP1570	TPPM0115
C5J1	STUFF 0.01UF	EMPTY
C5H5	STUFF 0.1UF	EMPTY
R5H3	EMPTY	STUFF 0-OHM

+12V
R6J6 2.2 5% CH 805
C6J6 1UF 20% 16V X5R 805
VREG_TPPM0115_VCC_PU
U6J1 TPPM0115 IC
VCC DRVH PWRGD PHASE TEST DRVL SEN GND
TP_PWRGD_V2P5
TEST_PIN3
VREG_2P5_PN1
VREG_FETGATE_MEM_PN2
C6J1 .01UF 10% 50V EMPTY 603
C6H5 .1UF 10% 16V EMPTY 603
VCC
L6J1 1.7UH IND
V_5P0_FILTER_2P5SM
C6H4 4.7UF 20% 10V Y5V 1206
C7H8 4.7UF 20% 10V Y5V 1206
C6H3 .1UF 10% 16V X7R 603
C7H4 2200UF 20% 16.0V ALUMINUM RDL
C6H1 2200UF 20% 16.0V ALUMINUM RDL
PHD55N03LT Q6H1 740985-001 FET
R6H1 0 805 1A CH
R6H3 0 603 1A CH
VREG_2P5_MEM_PN1
L6H1 4UH IND
V_2P5_CORE OUT 9 13 68
C5H1 1500UF 20% 6.3V ALUM RDL
C5G20 4.7UF 10% 10V X5R 1206
PHD55N03LT Q6H2 740985-001 FET
R6H4 0 805 1A CH
R6H2 2.2 5% CH 805
C6H2 4700PF 20% 50V X7R 603
VREG_3P5_MEM_PN2
68 IN VMARG_2P5_MEM
R6J2 1.5K 603 1% CH
54 IN VREG_USB_NCH_L
54 IN VREG_USB_PCH_L
U5H1 FET
R6J5 1.5K 603 1% EMPTY
R6J4 1K 1% CH 603
Q5G1 MOSFET
V_2P5_SM OUT 9 10 13 52 57
C5H2 1500UF 20% 6.3V ALUM RDL
C5G19 4.7UF 10% 10V X5R 1206
C5H3 1UF 10% 10V X5R 603

2.5VSTBY REGULATOR

ADJ Q4G1 MC33269
46 44 27 26 53 56 55 54 48 IN V_5P0_STBY
IN OUT ADJ SM
V_2P5_SM_SRC
C4H2 1UF 20% 25V Y5V 603
C5J2 330UF 20% 2.5V TANTALUM RDL
C4H1 1UF 20% 25V Y5V 603
R4G2 453 1% CH 603
R4G1 453 603 1% CH
C4G5 .1UF 20% 25V Y5V 603
C5G21 100UF 20% 6.3V X5R 1812

2.5V DDR REGULATOR

DRAWING
855GMEFB.SCH_1.51
Wed Apr 13 15:33:05 2005

INTEL CORPORATION 5200 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	51	C3

ROOM=DCL_DDR_VR

57 13 10 9 51 IN

V_2P5_SM

+12V

R7H7 10 5% CH 603

C7H5 1UF 10% 10V X7R 603

INV_A_PIN8

U7H1 LM358 IC

INV_A_OUT

INV_A_PIN4

R7H3 10 603 5% CH

+12V

C7H2 1UF 10% 10V X7R 603

BAT54C SOT23C DIO

Q7H1

U7G1 FET MTD3302

R7H1 49.9 1% CH 603

R7G1 1K 603 5% CH

INV_A_UTT

R7H4 0 603 1A CH

R7H2 49.9 1% CH 603

C7H3 1.0UF 10% 10V Y5V 603

R7H6 0 1A EMPTY 603

V_1P25_MEMUTT

OUT 14 15 16

C7G17 470UF 20% 10V ALUM RDL

C8G2 470UF 20% 10V ALUM RDL

C7G11 .1UF 10% 16V X7R 603

U7G2 MOSFET A61801-001

C8G12 470UF 20% 10V ALUM RDL

C7G16 470UF 20% 10V ALUM RDL

U7H1 LM358 IC

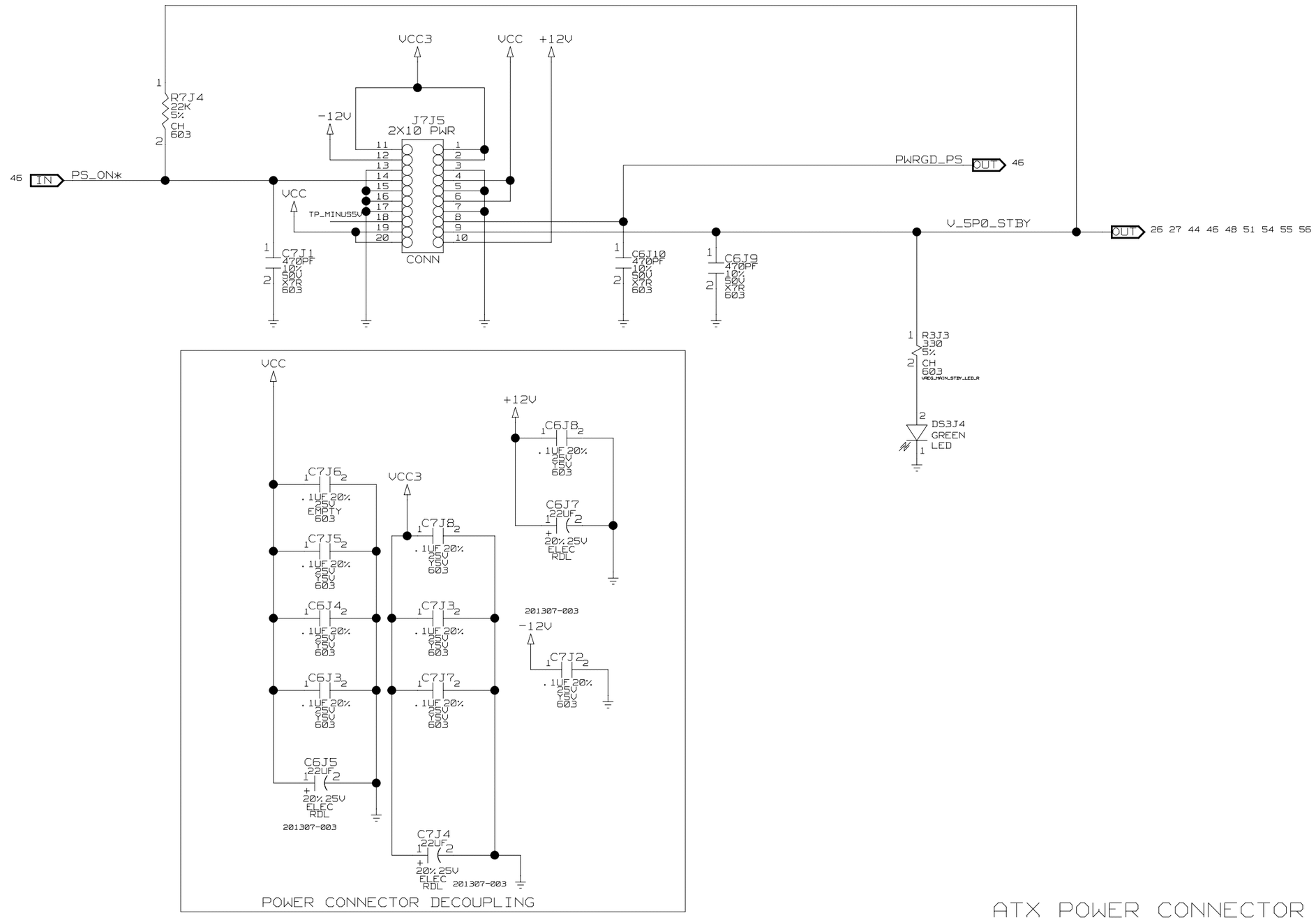
R7H5 0 603 1A EMPTY

DIMM_VREF_1P25

OUT 13 68 7

1.25V DDR REGULATOR

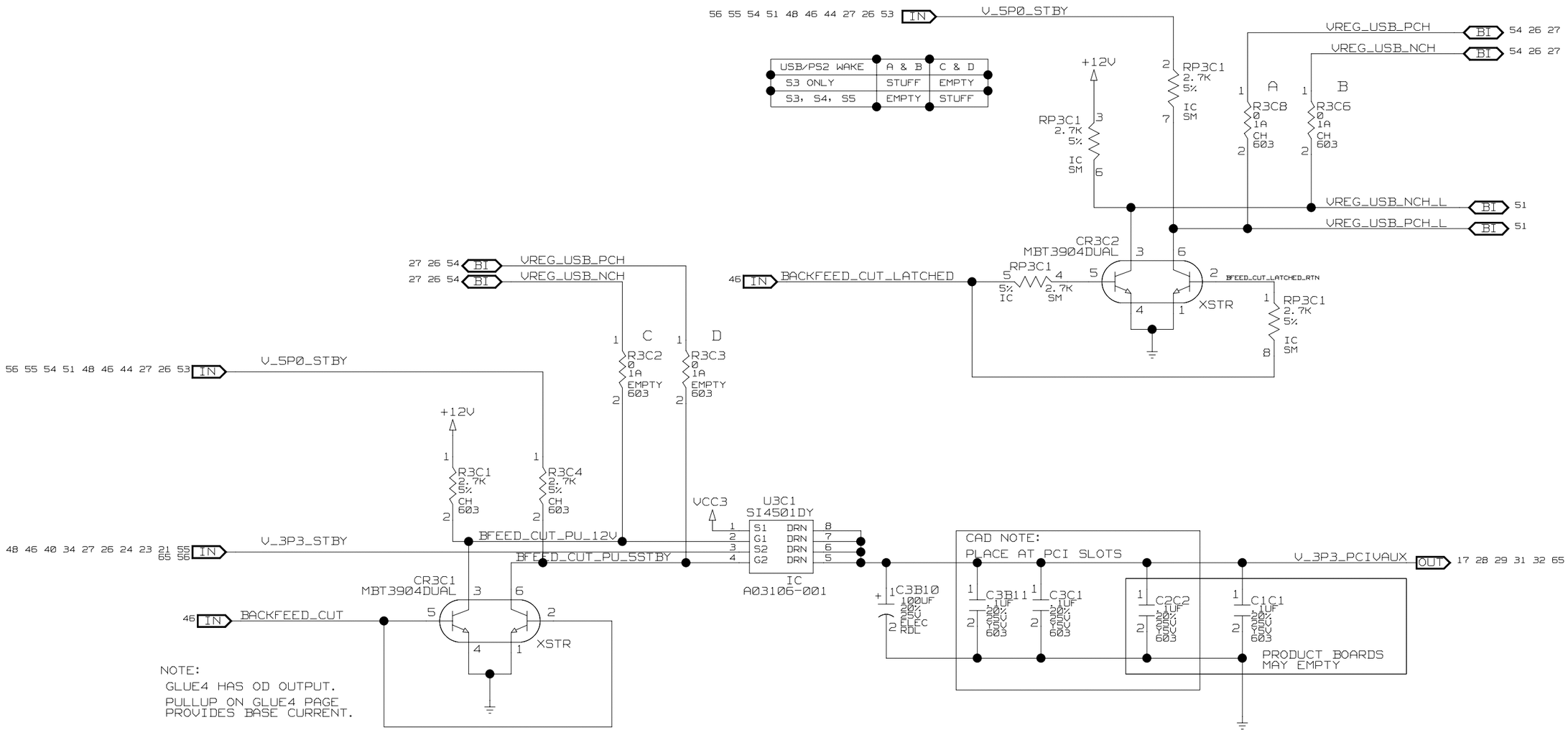
DRAWING				
855GMEFB.SCH_1.52 Wed Apr 13 15:33:06 2005	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 52	REV C3



ATX POWER CONNECTOR

DRAWING
855GMEFB.SCH_1.53
Wed Apr 13 15:33:06 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	53	C3

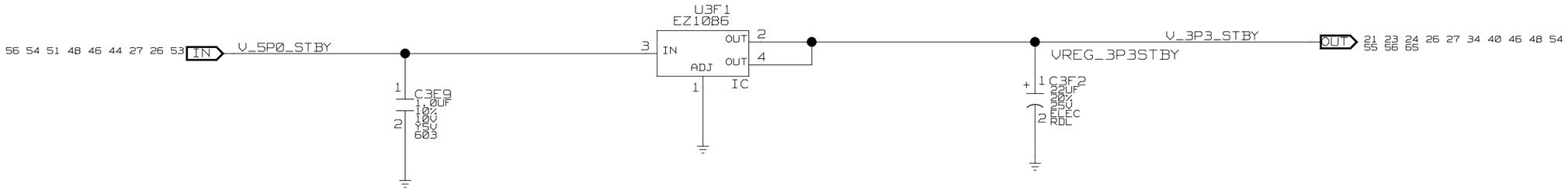


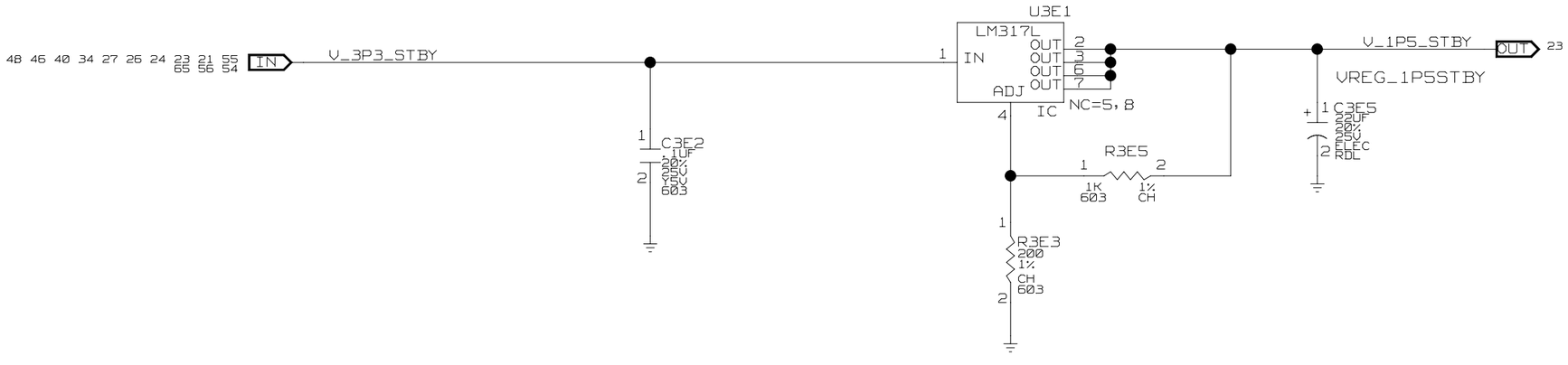
PCI VAUX

DRAWING
855GMEFB.SCH_1.54
Wed Apr 13 15:33:06 2005

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

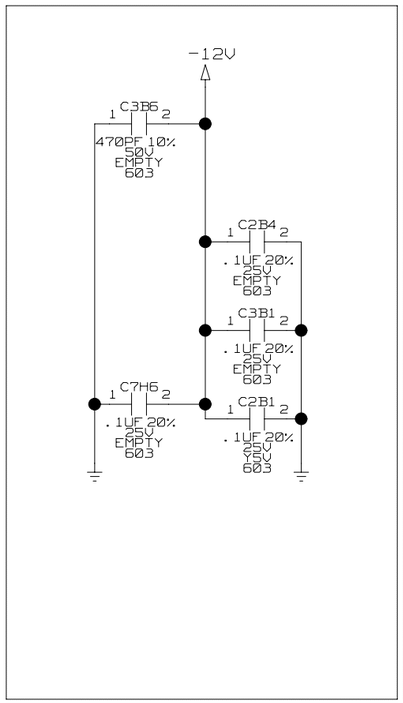
DOCUMENT NUMBER	PAGE	REV
30117601	54	C3

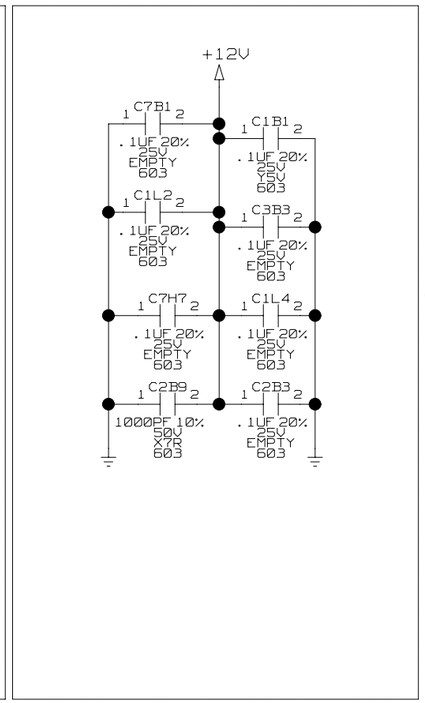


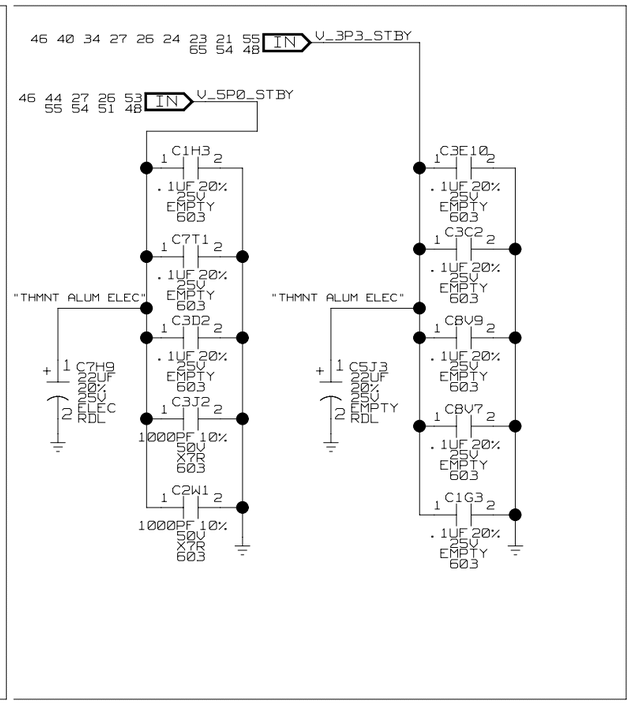


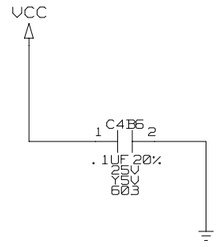
3.3V/1.5V STANDBY

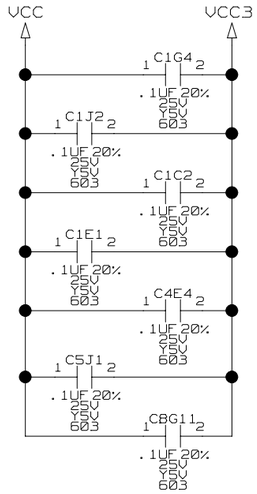
DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.55 Wed Apr 13 15:33:06 2005	5200 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	55	C3

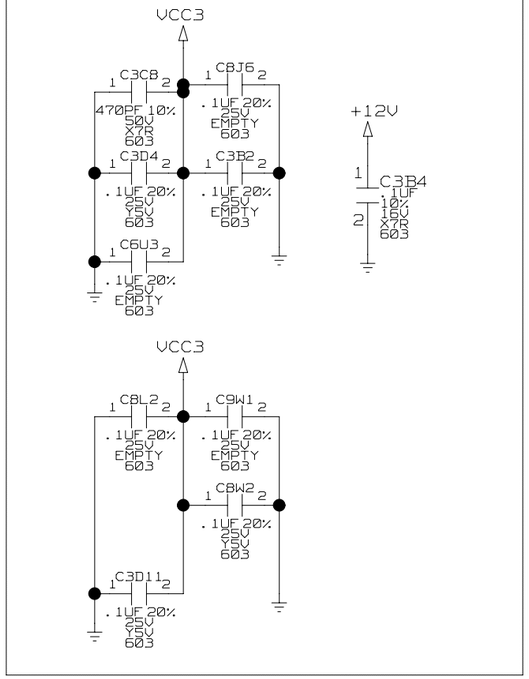


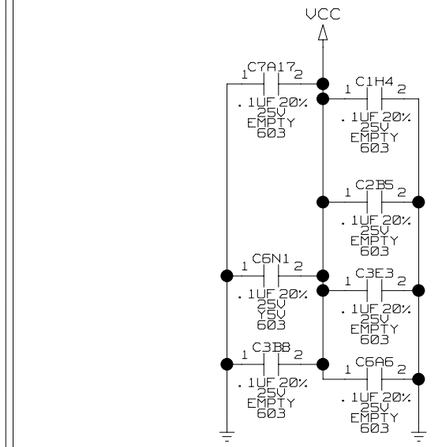


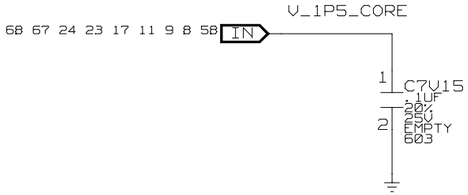


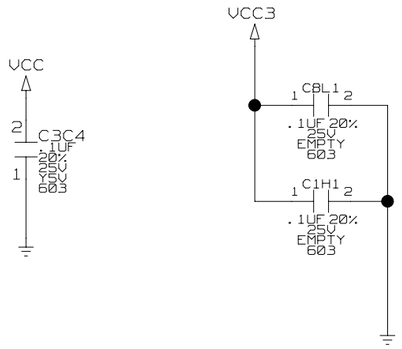


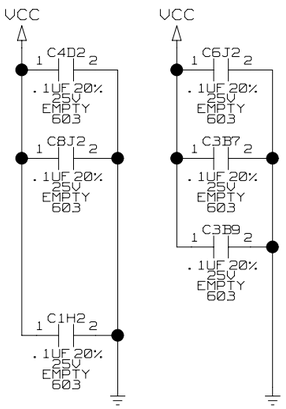


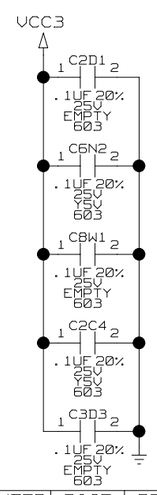








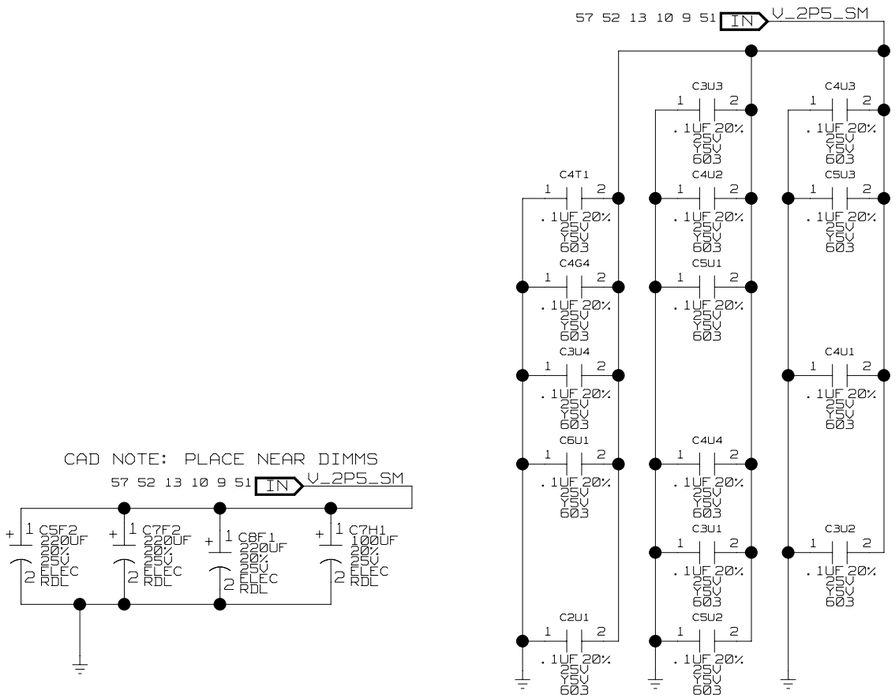




BULK DECOUPLING

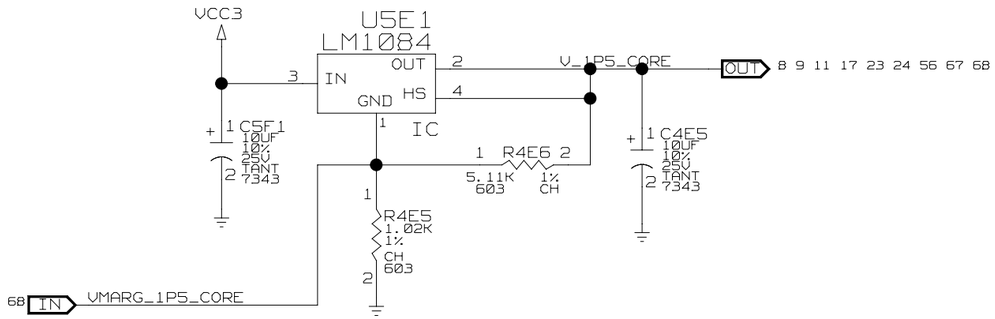
DRAWING
855GMEFB.SCH_1.56
Wed Apr 13 15:33:07 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	56	C3

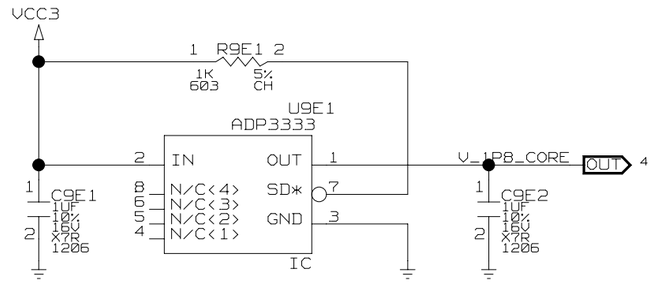


DDR 2P5_SM DECOUPLING

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEF B.SCH_1.57 Wed Apr 13 15:33:07 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	57	C3



CPU PLL POWER SUPPLY



1.5V & 1.8V REGULATOR

DRAWING
855GMEFB.SCH_1.58
Wed Apr 13 15:33:08 2005

INTEL CORPORATION 5200 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	58	C3

VCC3 VCC +12V

60 IN VDC_PHASE1

67 60 IN H_VID<5..0> 5 4 3 2 1 0

60 IN VDC_PHASE2

GMCH_VR_PWRGD IN 61

CPU_VR_PWRGD OUT 3 8

CPU_VR_DPWRGD OUT 24 21

CPU_CORE OUT 5 60

CPU_CORE

1 R8B1 2
0 1A
805 CH

CPU CORE REGULATOR

DRAWING
855GMEFB.SCH_1.59
Wed Apr 13 15:33:08 2005

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	59	C3

ROOM = DCL_CORE_CPU_VREG

MID FREQUENCY CPU DECOUPLING

5 59 IN CPU_CORE

C2P4 10.0UF 20% 6.3V X5R 805
C2P3 10.0UF 20% 6.3V X5R 805
C2P2 10.0UF 20% 6.3V X5R 805
C2P1 10.0UF 20% 6.3V X5R 805
C1P5 10.0UF 20% 6.3V X5R 805
C1P4 10.0UF 20% 6.3V X5R 805
C1P3 10.0UF 20% 6.3V X5R 805
C1P2 10.0UF 20% 6.3V X5R 805
C2N1 10.0UF 20% 6.3V X5R 805
C1P6 10.0UF 20% 6.3V X5R 805
C2P17 10.0UF 20% 6.3V X5R 805
C2P16 10.0UF 20% 6.3V X5R 805
C2P15 10.0UF 20% 6.3V X5R 805
C2P14 10.0UF 20% 6.3V X5R 805
C2P13 10.0UF 20% 6.3V X5R 805

C1P15 10.0UF 20% 6.3V X5R 805
C1P14 10.0UF 20% 6.3V X5R 805
C1P13 10.0UF 20% 6.3V X5R 805
C2N10 10.0UF 20% 6.3V X5R 805
C2P12 10.0UF 20% 6.3V X5R 805
C2P6 10.0UF 20% 6.3V X5R 805
C1P12 10.0UF 20% 6.3V X5R 805
C2P9 10.0UF 20% 6.3V X5R 805
C1P9 10.0UF 20% 6.3V X5R 805
C2N11 10.0UF 20% 6.3V X5R 805
C1N1 10.0UF 20% 6.3V X5R 805
C2N8 10.0UF 20% 6.3V X5R 805
C2N7 10.0UF 20% 6.3V X5R 805
C2N6 10.0UF 20% 6.3V X5R 805
C2N4 10.0UF 20% 6.3V X5R 805
C2N5 10.0UF 20% 6.3V X5R 805
C2N3 10.0UF 20% 6.3V X5R 805
C2N2 10.0UF 20% 6.3V X5R 805
C1N2 10.0UF 20% 6.3V X5R 805
C2N9 10.0UF 20% 6.3V X5R 805

BULK CPU DECOUPLING

C8C2 220UF 20% 2.5V TANT 7343
C7C4 220UF 20% 2.5V TANT 7343
C8C1 220UF 20% 2.5V TANT 7343
C9C3 220UF 20% 2.5V TANT 7343

VCCP

VCCP CPU DECOUPLING

C2P5 1UF 5% 16V X7R 603
C2P8 1UF 5% 16V X7R 603
C2P7 1UF 5% 16V X7R 603
C2P11 1UF 5% 16V X7R 603
C2P10 1UF 5% 16V X7R 603
C1P10 1UF 5% 16V X7R 603
C1P7 1UF 5% 16V X7R 603
C1P1 1UF 5% 16V X7R 603
C1P8 1UF 5% 16V X7R 603
C1P11 1UF 5% 16V X7R 603
C8D1 150UF 20% 4V POSCAP 7343
C8D2 150UF 20% 4V EMPTY 7343

PLACE ON BOTTOM OF CPU UNDER BANIAS SOCKET CAVITY

VCCP

59 67 OUT H_VID<0> R8E6 1K 603 5% CH
59 67 OUT H_VID<1> R8E5 1K 603 5% CH
59 67 OUT H_VID<2> R8E4 1K 603 5% CH
59 67 OUT H_VID<3> R8E3 1K 603 5% CH
59 67 OUT H_VID<4> R8E2 1K 603 5% CH
59 67 OUT H_VID<5> R8E1 1K 603 5% CH

CPU VR FET DRAIN VOLTAGE

+12V
R9B6 0.002 2512 5%
VDC_PHASE1 OUT 59
C9B3 10UF 20% 25V X5R 1210
C9B4 10UF 20% 25V X5R 1210
C9C1 10UF 20% 25V X5R 1210
C9B5 10UF 20% 25V X5R 1210
C9C2 10UF 20% 25V X5R 1210

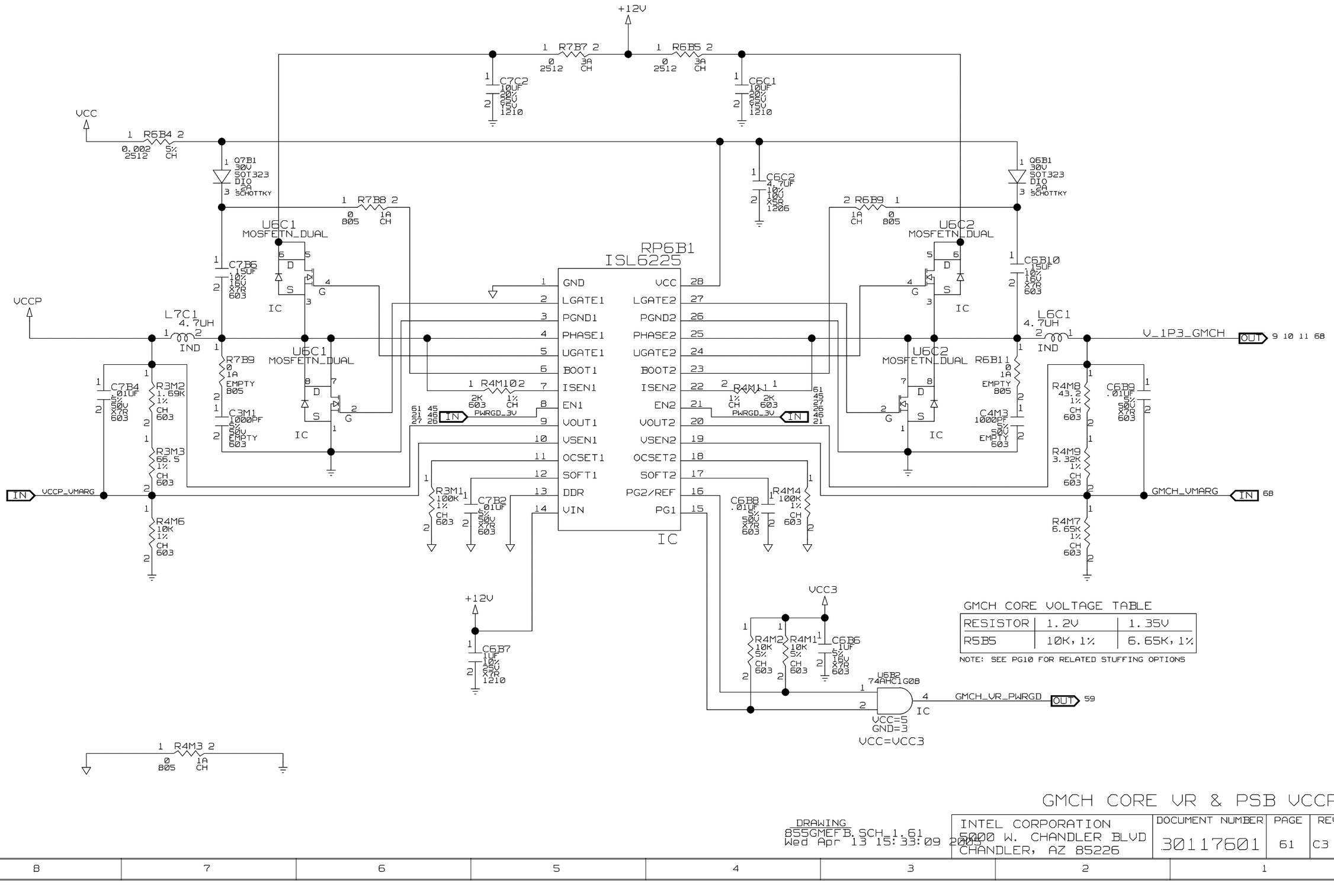
+12V
R7B6 0.002 2512 5%
VDC_PHASE2 OUT 59
C7B5 10UF 20% 25V X5R 1210
C7B3 10UF 20% 25V X5R 1210
C7C1 10UF 20% 25V X5R 1210
C7B7 10UF 20% 25V X5R 1210
C7C3 10UF 20% 25V X5R 1210

CPU DECOUPLING

DRAWING
855GMEFB.SCH_1.60
Wed Apr 13 15:33:08 2005

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	60	C3



GMCH CORE VOLTAGE TABLE

RESISTOR	1.2V	1.35V
R5B5	10K, 1%	6.65K, 1%

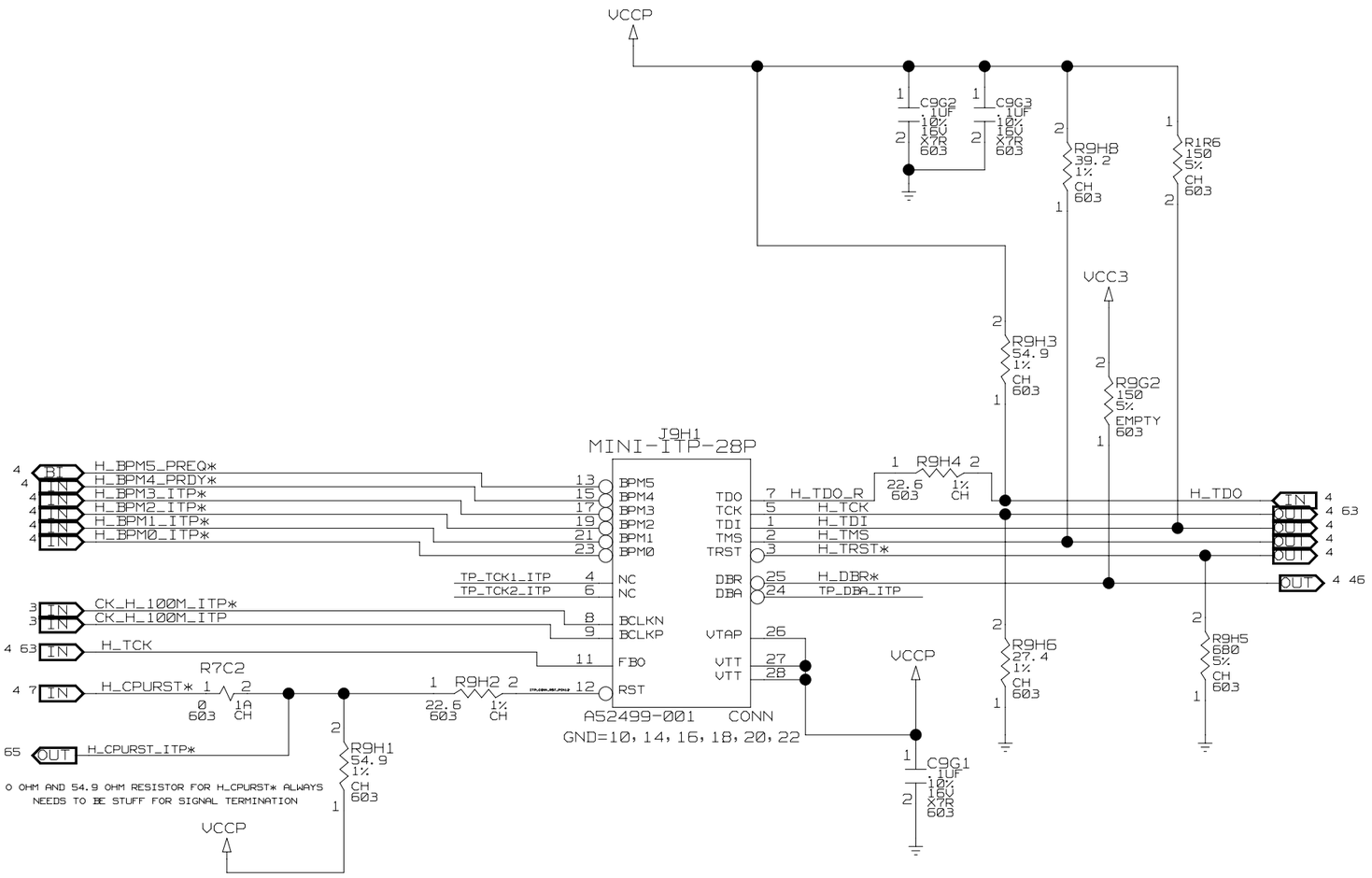
NOTE: SEE PG10 FOR RELATED STUFFING OPTIONS

GMCH CORE VR & PSB VCCP

DRAWING
855GMEFB.SCH_1.61
Wed Apr 13 15:33:09 2005

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	61	C3

DEBUG PAGES



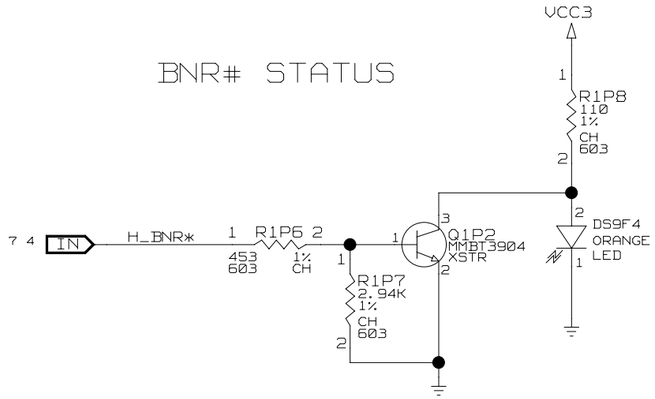
CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN. FBO LENGTH = TCK + BPM LENGTHS TO CPU.

SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

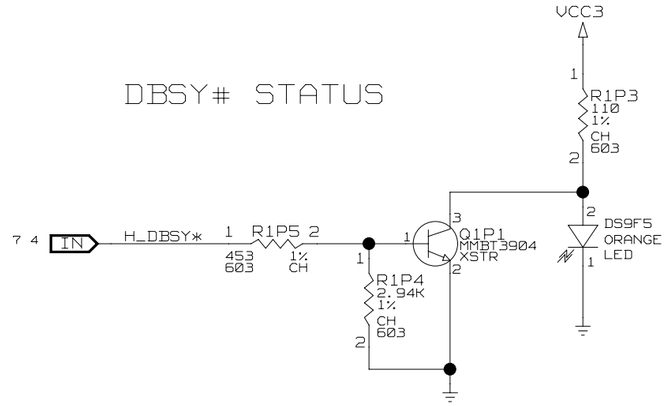
ITP 700FLEX CONNECTOR

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.63 Wed Apr 13 15:33:09 2005	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	63	C3

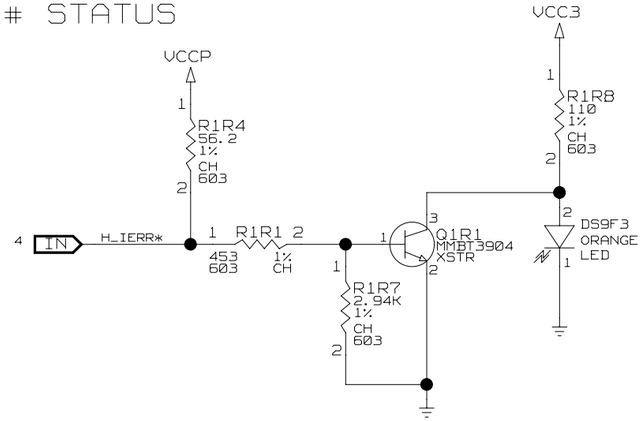
BNR# STATUS



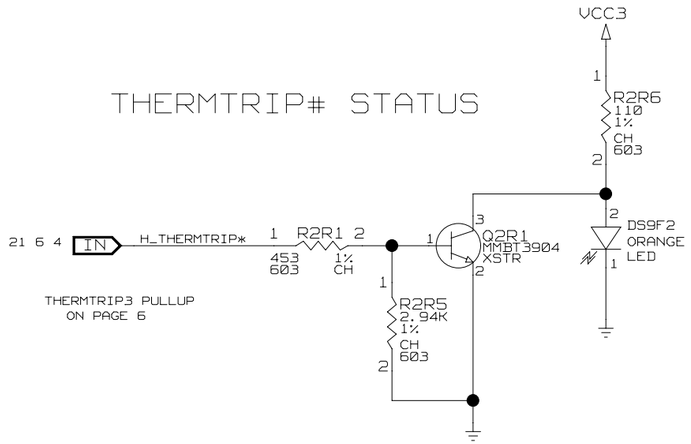
DBSY# STATUS



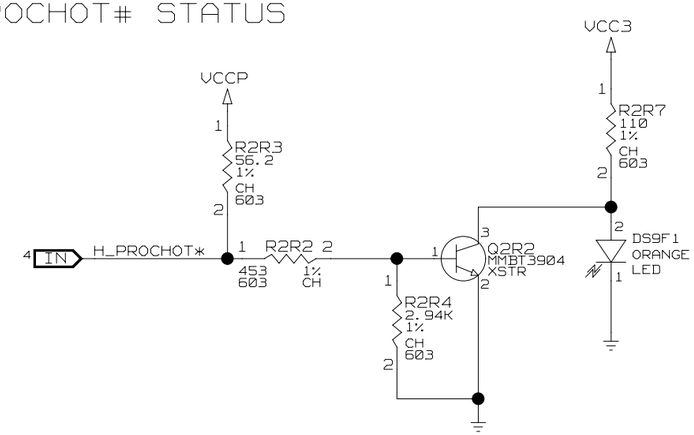
IERR# STATUS



THERMTRIP# STATUS



PROCHOT# STATUS

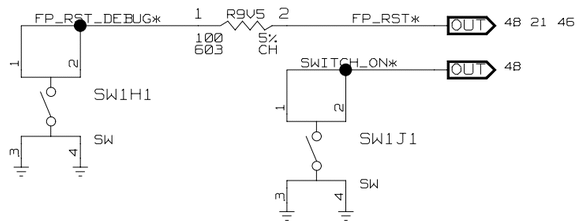


CPU STATUS LEDS

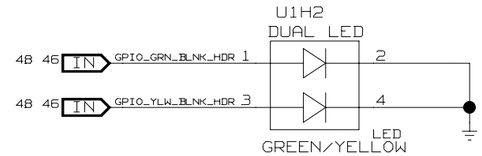
DRAWING
855GMEFB.SCH_1.64
Wed Apr 13 15:33:10 2005

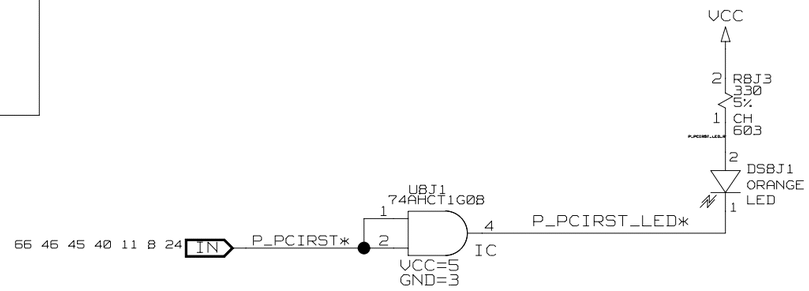
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	64	C3

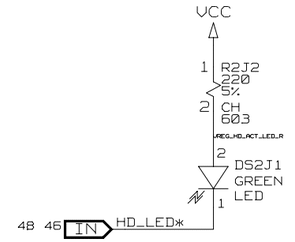
DEBUG/EV FEATURE: FRONT PANEL SWITCHES



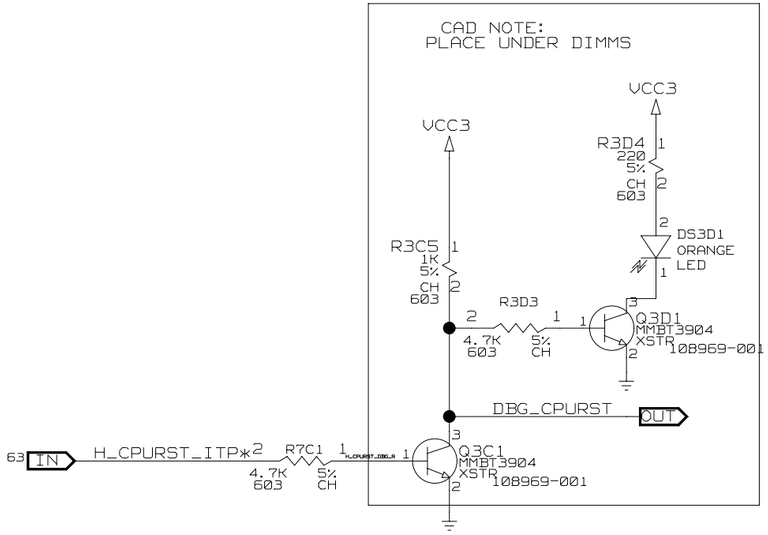
PRODUCT FEATURE: STATUS LED'S



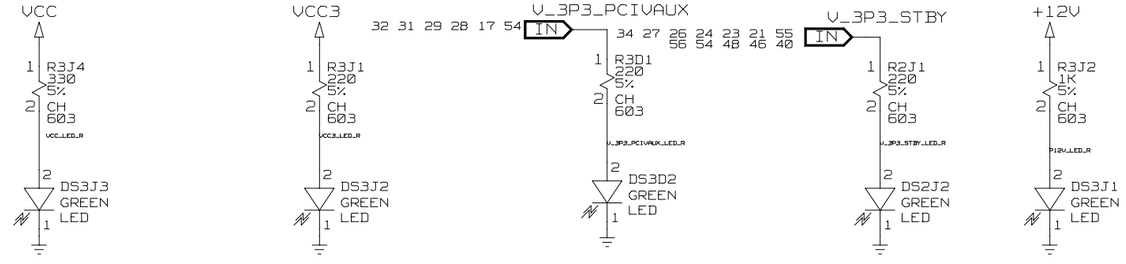




DEBUG/EV FEATURE: INVERTING LEVEL SHIFTERS ON FSB SIGNALS FOR DIAG LED'S



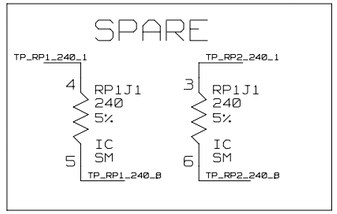
DEBUG/EV FEATURE: POWER RAIL STATUS LED'S



DEBUG STUFFING OPTIONS: BOM=VREG_LED_DEBUG

DEBUG LEDS, PWR/RST BTNS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.65 Wed Apr 13 15:33:10 2005	5200 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	65	C3

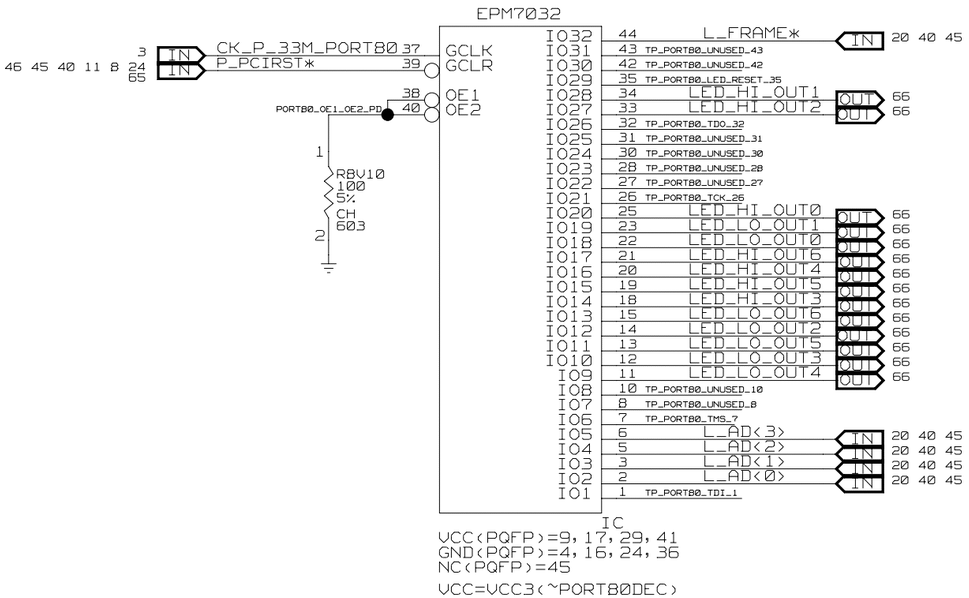


EPM7032AETC44-10

44 PIN TQFP

U2J1

EPM7032

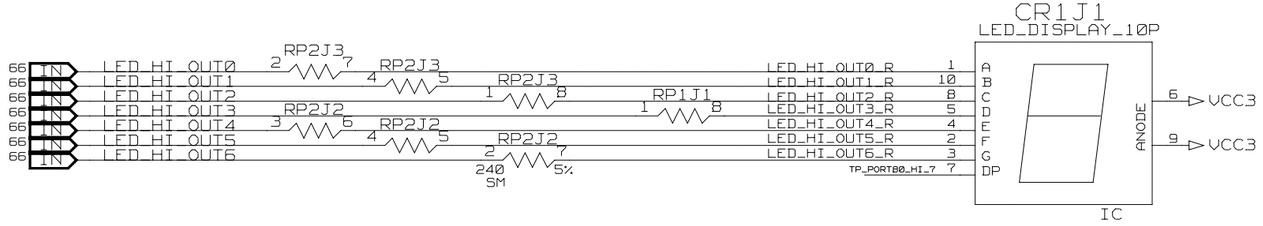


VCC(PQFP)=9,17,29,41
GND(PQFP)=4,16,24,36
NC(PQFP)=45
VCC=VCC3(~PORT80DEC)

CAD NOTE: ORIENT TO LEFT

CR1J1

LED_DISPLAY_10P

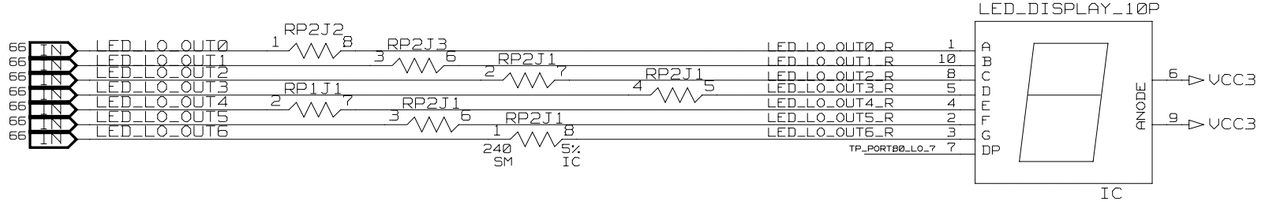


ALL RPACKS 240 OHMS

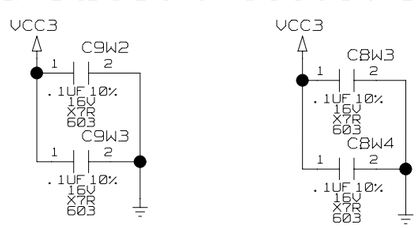
CAD NOTE: ORIENT TO RIGHT

CR2J1

LED_DISPLAY_10P



CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY



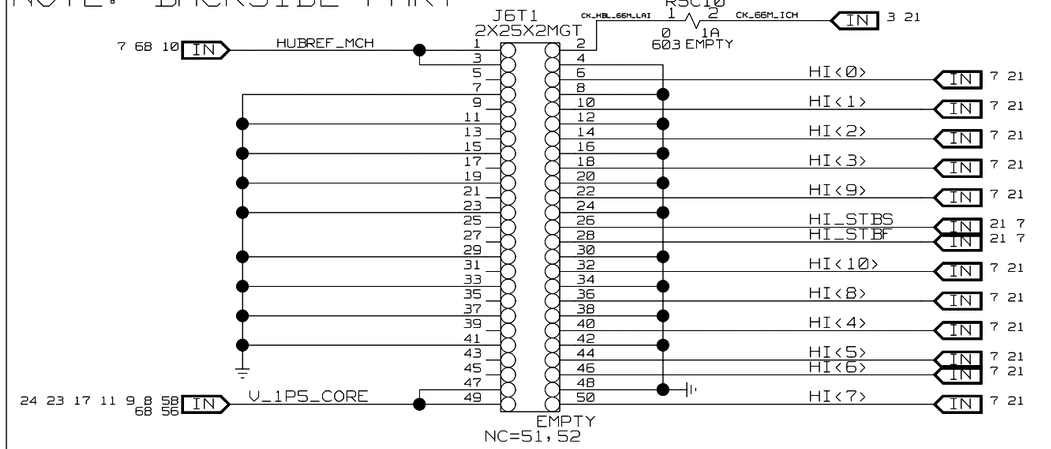
PORT 80 DECODER

DRAWING				
855GMEFB.SCH_1.66 Wed Apr 13 15:33:11 2005	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 66	REV C3

DEBUG/EV FEATURE: HUBLINK LAI HEADER

NOTE: BACKSIDE PART 700000-450

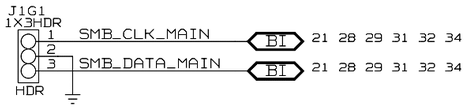
PLACE AT MIDPOINT OF HUBLINK ROUTING



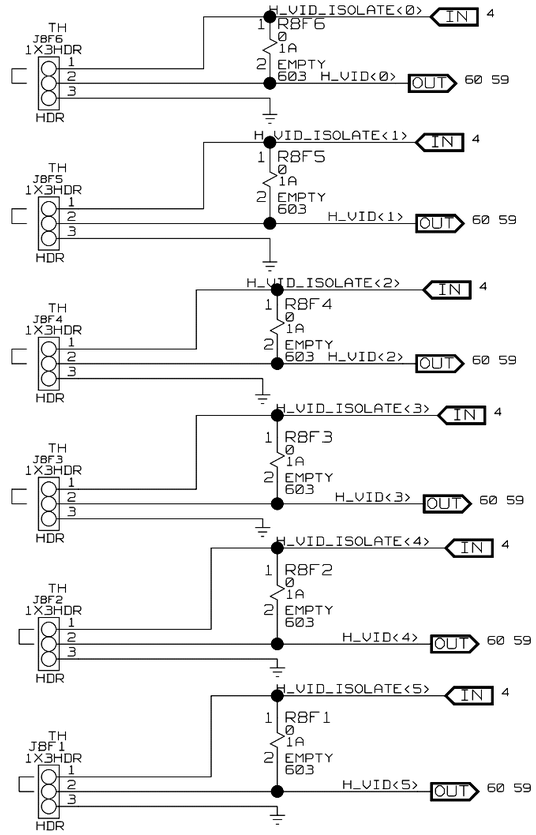
SOLDER MASK PADS: 5, 9, 13, 17, 21, 25, 27, 31, 35, 39, 43, 45

PINS ARE NOT ASSIGNED TP SIGNAL NAMES (PREVENTS TRACE CONNECTION)

DEBUG/EV FEATURE: SMBUS LAI HEADER

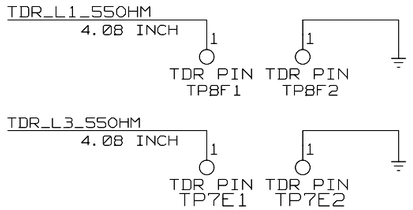


DEBUG/EV FEATURE: VID JUMPERS



VID 5	4	3	2	1	0	VCORE	VID 5	4	3	2	1	0	VCORE
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

DEBUG/EV FEATURE: TDR COUPONS

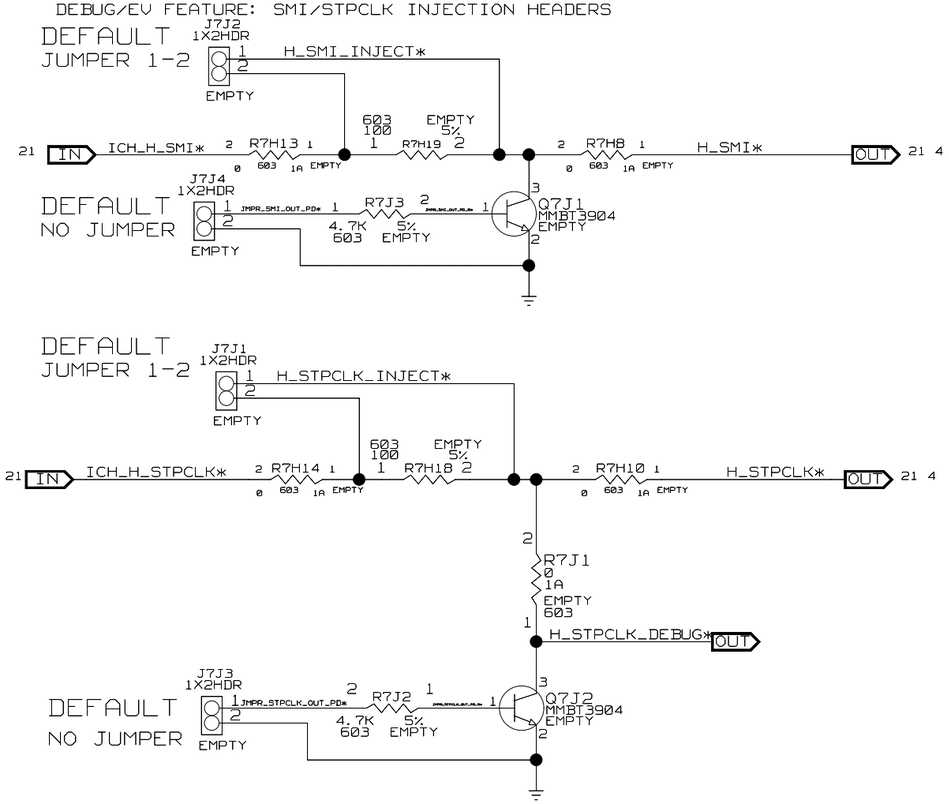


HI PROBE, SMB/VID JUMPERS, TDR

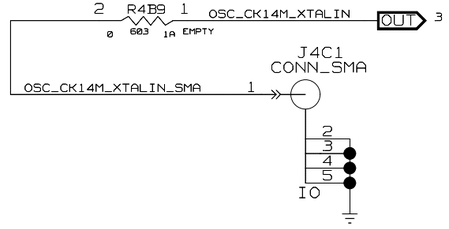
DRAWING
855GMEFB.SCH_1.67
Wed Apr 13 15:33:11 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	67	C3

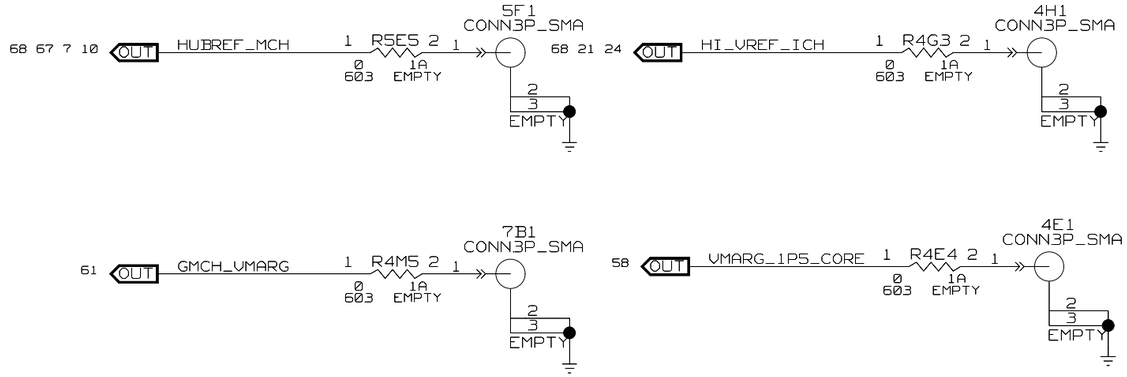
DEBUG/EV FEATURE: SMI/STPCLK INJECTION HEADERS

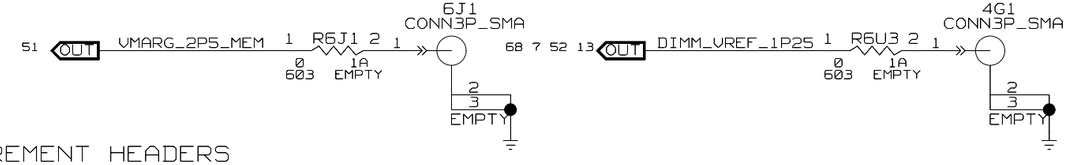


DEBUG FEATURE

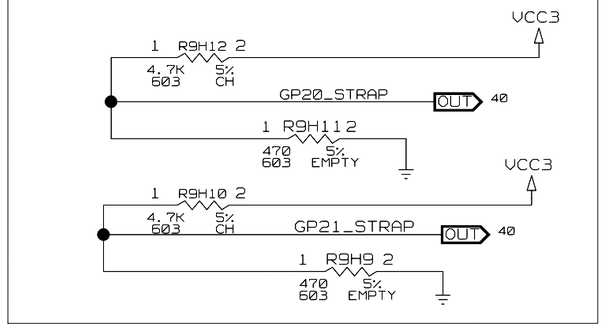


DEBUG/EV FEATURE: SMA MARGINING CONNECTORS

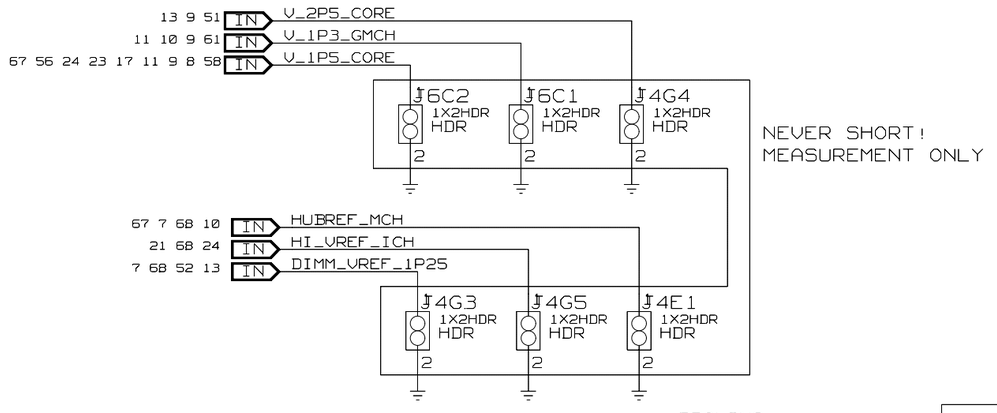




DEBUG/EV FEATURE: GPIO STRAPS



DEBUG/EV FEATURE: MEASUREMENT HEADERS



SMI/STPCLK INJECTION SMA CONNECTORS

DRAWING
855GMEFB.SCH.1.68
Wed Apr 13 15:33:11 2005

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	68	C3

REVISION HISTORY

REV C0

MADE PUBLIC VERSION
CHANGED TO BPAGE PUBLIC

REV C1

REMOVED OLD DOC NO.

REV C2

P24 CHANGED R7V8 FROM EMPTY 10K TO POPULATED 8.2K
PAGE 2 ADDED AGP 4X TO DVO BLOCK
PAGE 4 REMOVED NS NOTE
PAGE 11 UPDATED STRAPPING TABLE

REV C3

P3 CHANGED R5B5 FROM EMPTY TO POPULATED 330HM RESISTOR TO ENABLE AUDIO